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Application of inverter-grade thyristors in a single-phase forced-commutation inverter

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The operation of the single-phase two-thyristor parallel inverter using energy-recovery diodes is described, with particular reference to the waveforms obtained with inductive, resistive, and capacitive loads. From these waveforms the ratings of the thyristors required for safe and efficient working are derived. A practical trigger system is described, and a design example for a practical inverter given.

LIST OF SYMBOLS

The principal symbols used are listed below

C_c	commutation capacitance
I_{Cc}	current flowing in commutation capacitor
I_{CSR2}	current in thyristor CSR_2
I_{D2}	current in series diode D_2
I_{D4}	feedback current in energy-recovery diode D_4
I_{line}	d.c. line (supply) current
I_{load}	load current, in transformer secondary winding
I_{max}	maximum current during commutation cycle
L_1	commutation inductance
L_{2A}, L_{2B}	inductance to limit rate of rise of current
n	tapping ratio in transformer
t_c	commutation time of circuit
t_{off}	circuit turn-off time
V_{ak2}	voltage across thyristor, anode to cathode
V_b	d.c. supply voltage
V_{Cc}	voltage across commutation capacitor
V_{CSR2}	voltage from anode of thyristor to earth
$V_{(D2+CSR2)}$	voltage across thyristor and series diode, measured from anode of diode to earth
V_{D4}	voltage across energy-recovery diode, measured from cathode of diode to earth
V_{L1}	voltage across commutation inductor
τ_L	time-constant of commutation inductor
τ_p	time-constant of initial current rise at start of commutation with capacitive load

INTRODUCTION

A new range of thyristors has been recently introduced with characteristics especially suited for operation in a wide range of inverter circuits. One of the chief characteristics of the range is a fast turn-off time which allows commutation components to be reduced in value, thus enabling considerable cost savings to be made particularly in forced-commutation inverters. Another improved characteristic is the ability to withstand high rates of rise of current and voltage (high dI/dt and dV/dt ratings respectively).

To ensure efficient use of the thyristors in inverter circuits, certain dynamic properties of the thyristor should be matched closely to the operating properties of the inverter. In this article these properties of the thyristor are considered in relation to a standard single-phase two-thyristor inverter of the well-known 'McMurray' type. The commutation system of this type of inverter is similar to others such as the four-thyristor bridge and auxiliary-impulse types. These inverters operate normally at low to moderate frequencies in the range 50Hz to lkHz, and are widely used for standby power supplies and motor drive systems.

The operation of the two-thyristor inverter with energy-recovery diodes is taken as an example to indicate the use of thyristor characteristics to obtain reliable performance. In addition, a variable-frequency trigger system constructed from circuit modules to allow easy external wiring and assembly is described.

TYPE DESIGNATION AND CHARACTERISTICS

The new range of thyristors has two type numbers, BTW30 and BTW31. For squarewave operation they are rated at a mean current of 12 and 16A respectively. Brief data for the two types and the voltage grades available are listed in Table 1.

OPERATION OF INVERTER CIRCUIT

The basic inverter circuit shown in Fig. 1 is used to describe the waveforms produced with lagging, leading, and resistive loads. The waveforms are shown in Figs. 2 to 7. A nominal supply voltage of 80V was used for the waveforms with a commutation capacitance and inductance of 2µF and 2mH respectively. The transformer had an approximately 1 to 1 primary-to-secondary turns ratio.

TABLE 1

Brief Data for BTW30 and BTW31 Thyristors

		BTW30/ 300R	400R	500R	600R	800R	1000R	1200R	
V_{DWM} max.		300	400	500	600	600	700	800	V
V_{DRM} max.		300	400	500	600	800	1000	1200	V
V_{RRM} max.		300	400	500	600	800	1000	1200	V
$I_{T(AV)}$ max.	square wave, d = 0.5								
	$T_{mb} \leq 65^oC$	16							A
	$T_{mb} = 85^oC$	12							A
$I_{T(RMS)}$ max.		31							A
I_{TSM} max.	single square pulse, t = 5ms $T_j = 125^oC$ prior to surge	150							A
T_j max.		125							^oC
$\frac{dI_T}{dt}$ max.		100							A/µs
$\frac{dV_D}{dt}$ max.		200							V/µs
t_q max.	$T_j = 125^oC$	300R to 600R 6µs				800R to 1200R 12µs			

		BTW31/ 300R	400R	500R	600R	800R	1000R	1200R	
V_{DWM} max.		300	400	500	600	600	700	800	V
V_{DRM} max.		300	400	500	600	800	1000	1200	V
V_{RRM} max.		300	400	500	600	800	1000	1200	V
$I_{T(AV)}$ max.	square wave, d = 0.5								
	$T_{mb} \leq 65^oC$	22							A
	$T_{mb} = 85^oC$	16							A
$I_{T(RMS)}$ max.		31							A
I_{TSM} max.	single square pulse, t = 5ms $T_j = 125^oC$ prior to surge	225							A
T_j max.		125							^oC
$\frac{dI_T}{dt}$ max.		100							A/µs
$\frac{dV_D}{dt}$ max.		200							V/µs
t_q max.	$T_j = 125^oC$	300R to 600R 12µs				800R to 1200R 20µs			

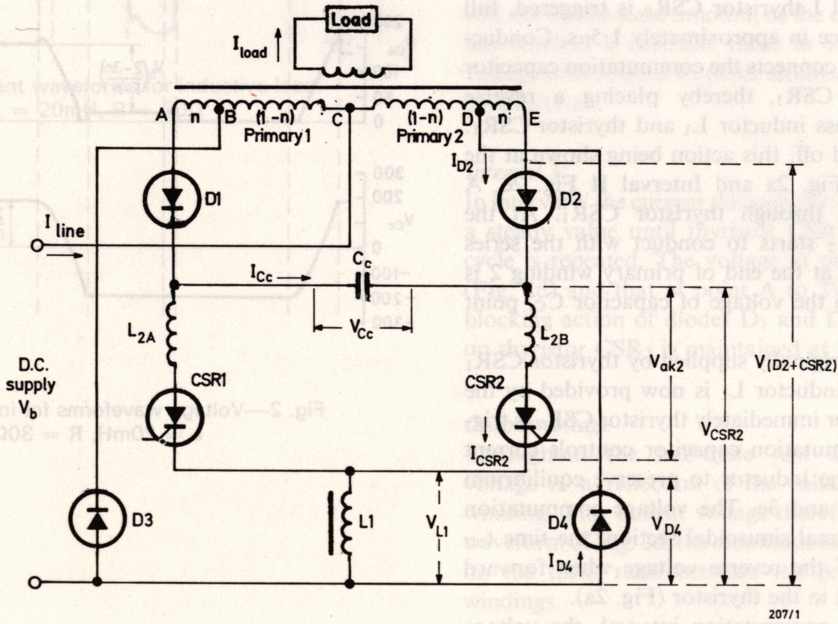

Fig. 1—Basic inverter circuit incorporating energy-recovery diodes

Inverter with inductive load

The inverter load was set at 20mH and 30Ω, and the operating frequency was approximately 300Hz. This gave a load power factor of about 0·6. The waveforms of Figs. 2 and 3 represent the voltage or current across a particular device, the symbols for each waveform corresponding to the symbols marked on the circuit diagram of Fig. 1. To make the commutation interval clearer, the time scale in the waveforms has been expanded over this interval to twice the value for the rest of the cycle. Because of the symmetrical operation of the inverter, it will be appreciated that sections VI to IX of the waveforms if transposed against sections II to V represent the voltage or current for the complementary device. To preserve continuity, interval I is the continuation of the right-hand end of the waveform.

Interval I

Thyristor CSR_1 is conducting and current is flowing into the load. For a moderate rate of change of current, the voltage across the commutation inductance L_1 is assumed to be zero. Also, in this interval the voltage on the right-hand side of the commutation capacitor C_C and the anode-to-earth voltage of thyristor CSR_2 reach a value $2V_b/(1-n)$ through autotransformer action in section CE of the transformer during the preceding half-cycle and the blocking action of the series diodes D_1 and D_2. This is shown in Figs. 2b and 2f.

Interval II (commutation interval)

At the end of interval I thyristor CSR_2 is triggered, full conduction taking place in approximately 1·5μs. Conduction in thyristor CSR_2 connects the commutation capacitor C_C across thyristor CSR_1, thereby placing a reverse voltage $2V_b/(1-n)$ across inductor L_1 and thyristor CSR_1. The thyristor is turned off, this action being shown at the start of Interval VI Fig. 2a and Interval II Fig. 2c. A reverse current flows through thyristor CSR_1. At the instant thyristor CSR_2 starts to conduct with the series diode D_2, the voltage at the end of primary winding 2 is momentarily raised to the voltage of capacitor C_C, point S_1 on Fig. 2d.

The load current originally supplied by thyristor CSR_1 and flowing through inductor L_1 is now provided by the commutation capacitor immediately thyristor CSR_2 is triggered. Thus the commutation capacitor controls current for the load and in the inductor to preserve equilibrium as shown in Figs. 3b and 3e. The voltage commutation waveform has the normal sinusoidal section, the time t_{off} being the duration of the reverse voltage when forward blocking is established in the thyristor (Fig. 2a).

At the end of the commutation interval, the voltage across inductor L_1 reaches zero. Consequently the current in thyristor CSR_2 and inductor L_1 reaches a maximum value I_{max}. The voltage across the commutation capacitor reverses (that is, the charge reverses), Fig. 2f, and the anode of thyristor CSR_2 begins to swing negative with respect to earth to reach a value Vb.n/(1-n), Fig. 2b. A short time later the tap for the diode reaches zero voltage, Fig. 2e, and diode D_4 starts to conduct, discharging stored energy $\frac{1}{2}L_1I_x^2$ where I_x is a slightly reduced value of I_{max} caused by the time lag through the tapping ratio n of the transformer. The commutation interval is substantially complete.

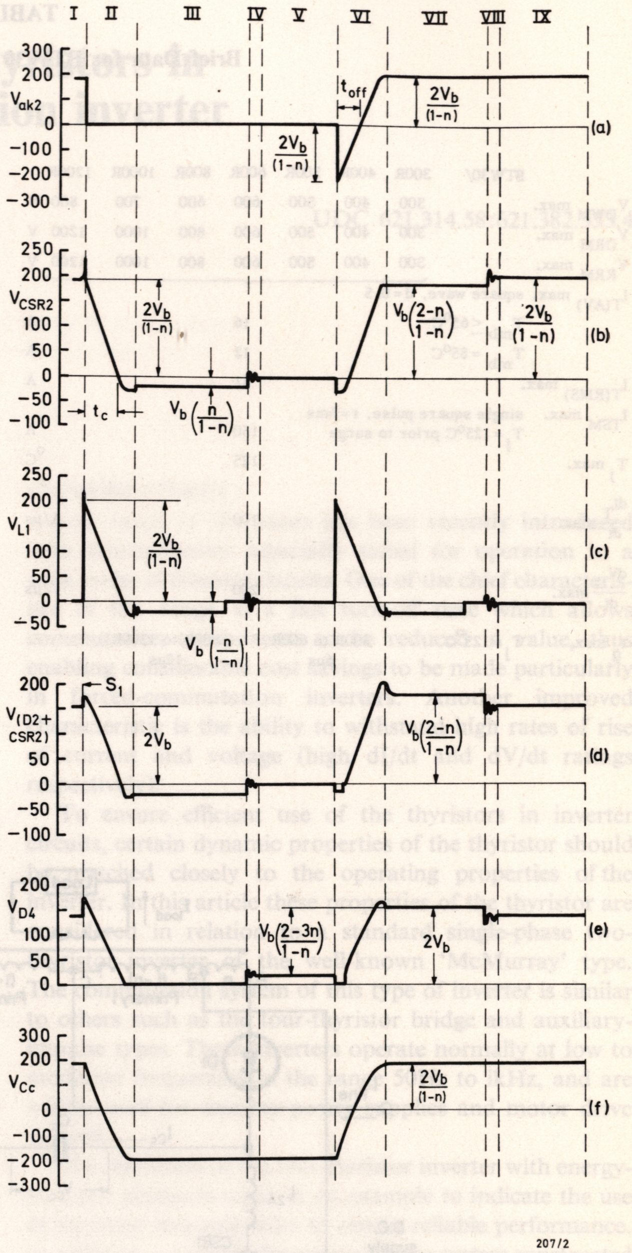

Fig. 2—Voltage waveforms for inductive load: L = 20mH, R = 30Ω

Interval III

With diode D_4 conducting, the voltage at the tapping point D of the transformer is zero. A common driving voltage is thus established between points D and E of primary winding 2 and the inductor L_1 of $-V_b.n/(1-n)$. The energy contained in the inductor is discharged with a time-constant τ_{L1} given by:

$$\tau_{L1} = \frac{L_1 I_{max}(1-n)}{nV_b} \text{ seconds.}$$

This discharge current circulates in winding DE and is transferred to winding CD and returned to the d.c. supply.

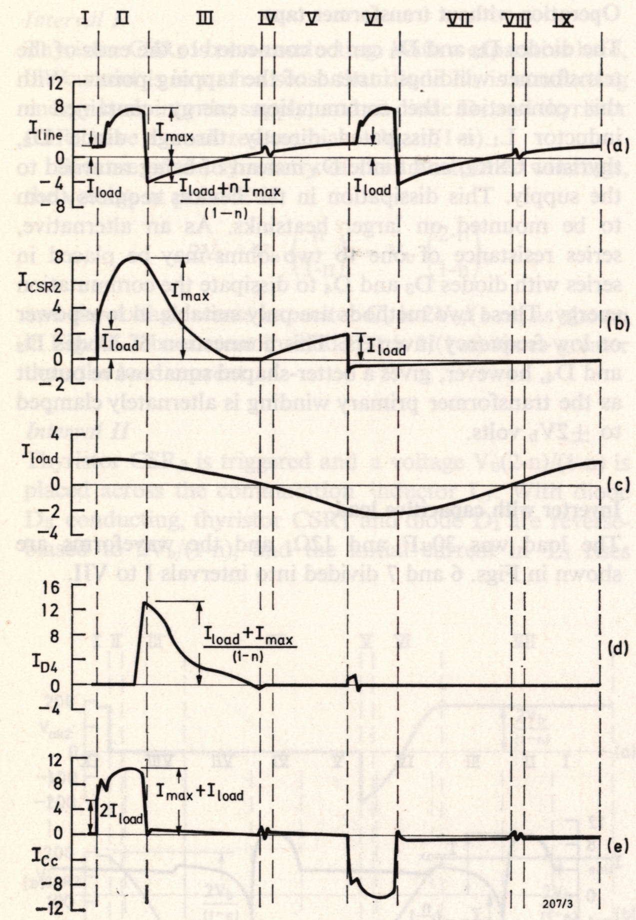

Fig. 3—Current waveforms for inductive load: L = 20mH, R = 30Ω

The voltage at point E is $-V_b.n/(1-n)$. Therefore by symmetry the voltage at point A and at capacitor C_C with respect to earth will be $V_b(2-n)/(1-n)$, giving the total voltage across the capacitor as $2V_b/(1-n)$. This is also the value of forward voltage applied to the non-conducting thyristor CSR_1.

After the energy contained in the inductor has been discharged, thyristor CSR_2 ceases conducting (Fig. 3b) but there is continuing feedback of energy from the inductive load until the polarity of the load current reverses, at which time diode D_4 ceases to conduct (Fig. 3d). This completes the third interval of the cycle.

Interval IV

At the start of interval IV a trigger pulse is required for thyristor CSR_2 to start conducting again, as described in the Trigger Pulse section following. If the build-up of current in inductor L_1 is not sufficiently rapid to supply the load, a proportion of the current is supplied by the commutation capacitor. This interchange between the commutation capacitor and inductor causes a ringing waveform of magnitude approximately $V_b.n/(1-n)$, as shown in Fig. 2c, gradually reducing in amplitude as the inductor provides the load current.

While diode D_4 is conducting, the voltage on the commutation capacitor is $V_b(2-n)/(1-n)$. When the diode ceases to conduct, the voltage at point E on primary winding 2 increases from $-V_b.n/(1-n)$ to zero. Hence the voltage on the left-hand side of the commutation capacitor will rise by the same amount, as the charge on the capacitor has reached a constant value in this interval. The final voltage with respect to earth attained by the capacitor will be $2V_b/(1-n)$.

Interval V

In interval V the current through thyristor CSR_2 approaches a steady value until thyristor CSR_1 is triggered and the cycle is repeated. The voltage at point E returns to zero (Fig. 2d) and that at point A to $2V_b$, but because of the blocking action of diodes D_1 and D_2 the forward voltage on thyristor CSR_1 is maintained at $2V_b/(1-n)$, Fig. 2b.

Output voltage

Throughout the half-cycle just described, the output voltage is a reflection of the voltage across the primary winding. The output voltage therefore follows closely the waveform of Fig. 2d, the amplitude being directly dependent on the turns ratio between the primary and secondary windings.

Trigger pulses

With an inductive load, as the load current is lagging the applied voltage, the conducting thyristor CSR_2 is switched off during the return of energy through diode D_4. Trigger pulses are therefore required to restart conduction in thyristor CSR_2 and to maintain a pick-up current condition during interval IV when the load current is being shared between the commutation capacitor and inductor L_1 during current build-up.

Inverter with resistive load

The inverter load was set at 20Ω and waveforms of the voltages and currents for particular components are shown in Figs. 4 and 5. The waveforms are divided into similar intervals as with the inductive load, the voltage waveforms having similar amplitudes.

As the load current is now in phase with the transformer secondary voltage, load current reversal takes place during the commutation interval. An extraction of energy from the inductor L_1 similar to that with the inductive load is shown in Fig. 5d, but the interval when diode D_2 returns load current to the supply is absent. With a resistive load, therefore, the thyristor conducts during the whole half-cycle, and the ringing waveform occurring with an inductive load in Intervals IV and VIII of Figs. 2 and 3 is absent. The half-cycle is completed with the thyristor conducting current to the load (Fig. 5b).

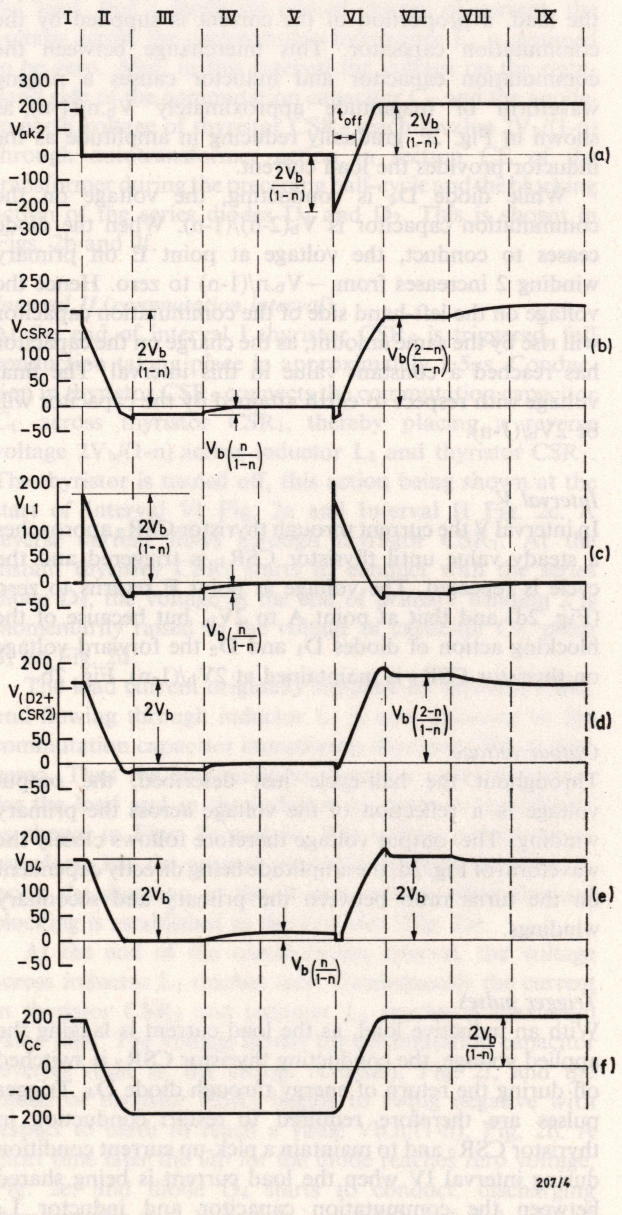

Fig. 4—Voltage waveforms for resistive load: R = 20Ω

Operation without transformer taps

The diodes D_3 and D_4 can be connected to the ends of the transformer windings instead of the tapping points. With this connection the commutation energy contained in inductor L_1 is dissipated directly through diode D_2, thyristor CSR_2, and diode D_4 instead of being returned to the supply. This dissipation in the devices requires them to be mounted on larger heatsinks. As an alternative, series resistance of one to two ohms may be placed in series with diodes D_3 and D_4 to dissipate the commutation energy. These two methods are only suitable in low-power or low-frequency inverters. This connection of diodes D_3 and D_4, however, gives a better-shaped squarewave output as the transformer primary winding is alternately clamped to $\pm 2V_b$ volts.

Inverter with capacitive load

The load was 30μF and 12Ω, and the waveforms are shown in Figs. 6 and 7 divided into intervals I to VII.

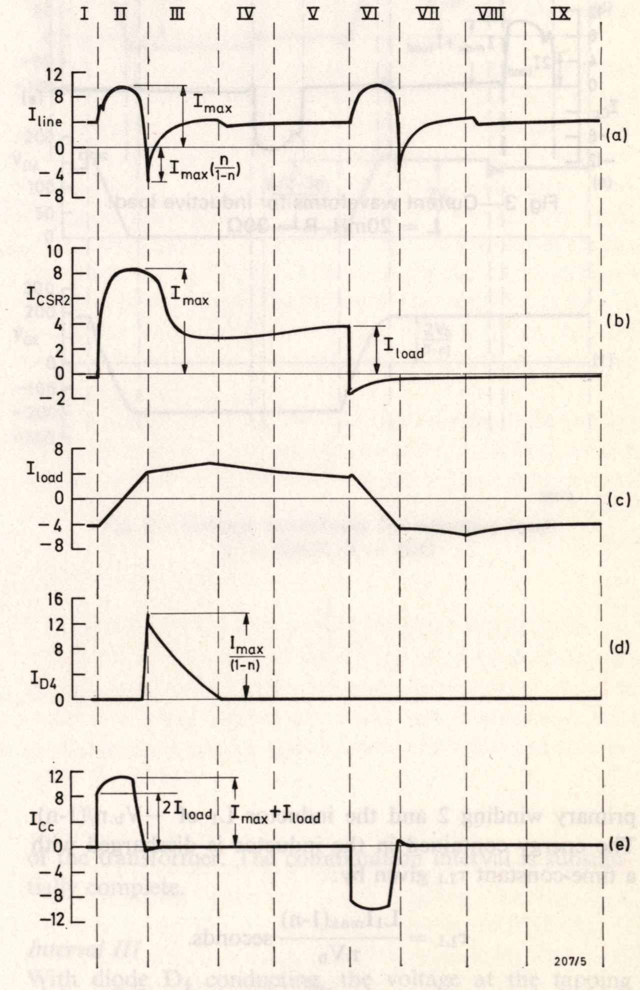

Fig. 5—Current waveforms for resistive load: R = 20Ω

Interval I

Thyristor CSR_2 is non-conducting. With a capacitive load, the current is in such a sense that diode D_3 is conducting energy back into the supply, and so diode D_1 and thyristor CSR_1 have a small reverse bias $-V_b.n/(1\text{-}n)$.

Because of the symmetry of the transformer windings, the voltage at point E is:

$$2V_b+V_b\left(\frac{n}{1\text{-}n}\right) = V_b\left(\frac{2\text{-}n}{1\text{-}n}\right),$$

and the voltage across capacitor C_c is $2V_b/(1\text{-}n)$, as shown in Fig. 6f. The current in diode D_3 is $1/(1\text{-}n)$ times greater than the load current.

Interval II

Thyristor CSR_2 is triggered and a voltage $V_b(2\text{-}n)/(1\text{-}n)$ is placed across the commutation inductor L_1. With diode D_3 conducting, thyristor CSR_1 and diode D_1 are reverse-biased to $2V_b/(1\text{-}n)$, and the initial current in L_1 rises linearly with a time-constant:

$$\tau_p = \frac{L_1.I_{load}(1\text{-}n)}{V_b(2\text{-}n)} \text{ seconds.}$$

This turn-off action of CSR_1 is superfluous as diode D_3 is conducting load current. Diode D_3 now ceases to conduct and effectively load current is transferred from D_3 to thyristor CSR_2.

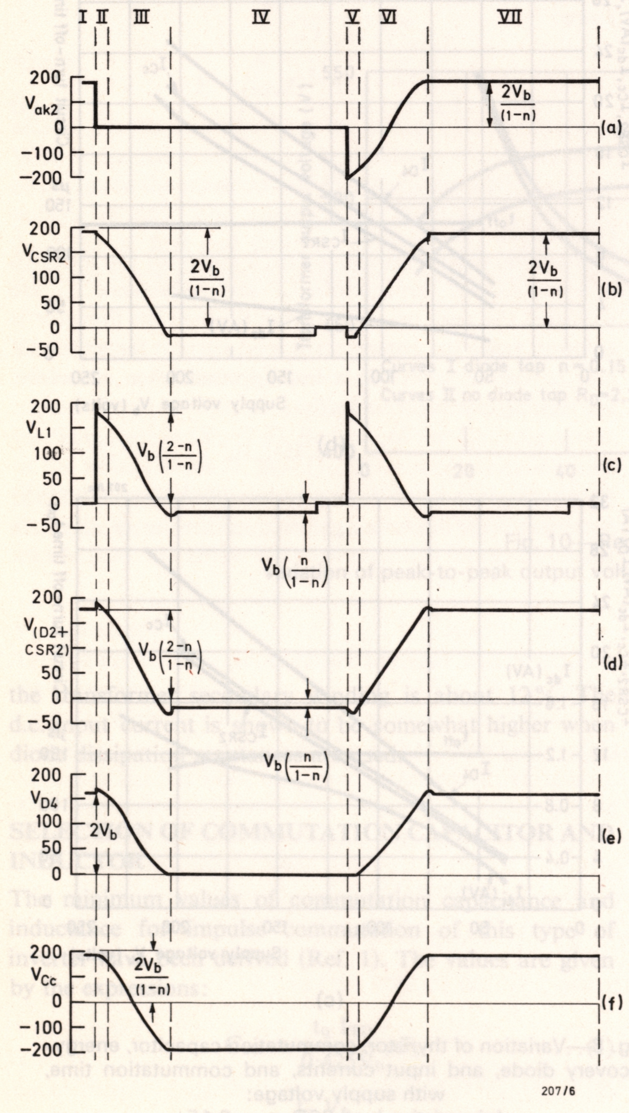

Fig. 6—Voltage waveforms for capacitive load: C = 30μF, R = 12Ω

Interval III

Interval III is the normal commutation transient as the commutation capacitor discharges into the inductor, the current reaching a maximum value I_{max} and the voltage transient being of a sinusoidal form.

When the current in thyristor CSR_2 reaches the maximum I_{max}, there is a short delay, and diode D_4 conducts to extract the energy from inductor L_1 into the supply through the tapped transformer. The voltage on the capacitor is raised to $2V_b/(1\text{-}n)$.

Interval IV

The current through thyristor CSR_2 and the inductor falls until it follows the load current, Figs. 7b and 7c. With diode D_4 conducting, the voltage from the anode of thyristor CSR_2 to earth falls to $-V_b.n/(1\text{-}n)$. Thyristor CSR_2 continues to conduct until the load current reverses, when diode D_4 continues to return load current to the supply.

Interval V

This interval is similar to interval II with diode D_4 conducting and thyristor CSR_1 on the point of being triggered.

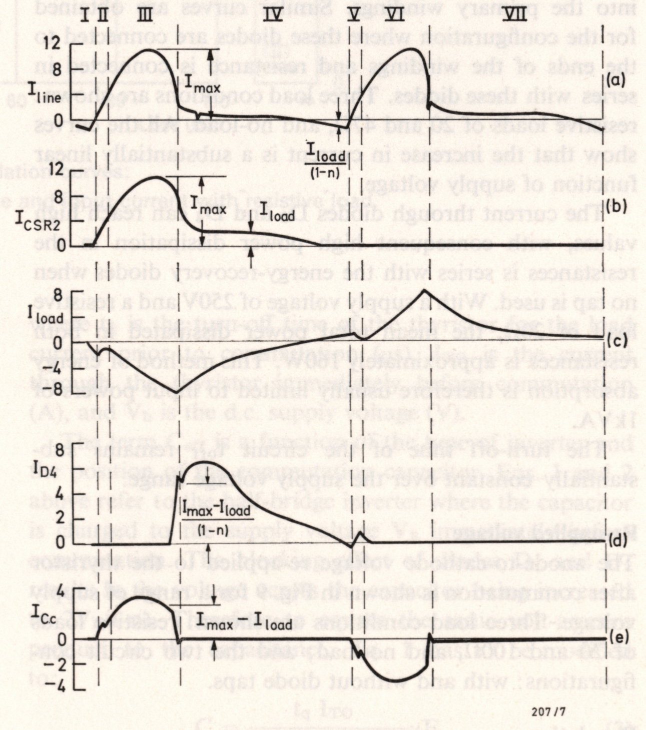

Fig. 7—Current waveforms for capacitive load: C = 30μF, R = 12Ω

Inverter with no load

When the inverter is operated under no-load conditions, the highest peak current is produced through the conducting thyristor for a given supply voltage, as shown in Figs. 8a, 8b, and 8c. The curves in these figures will be described in the next section. The highest current occurs at no-load because the commutation capacitor supplies only a small load current during the commutation interval.

In the no-load case the highest positive voltage is again $2V_b/(1\text{-}n)$.

PRACTICAL MEASUREMENTS

The waveforms of Figs. 2 to 7 were obtained with a d.c. supply voltage of 80V. Further measurements were made of the variation of certain peak currents in the inverter with changes of supply voltage, of the variation in the voltage re-applied to the thyristor after commutation with supply voltage, and of regulation.

Variation of peak currents with supply voltage

The variation with supply voltage of four currents in the inverter was measured and the results plotted in Fig. 8. The four currents are:

peak current through thyristor CSR_2 during commutation, I_{CSR2},
peak current through commutation capacitor C_c, I_{Cc},
peak current through diode D_4 during commutation, I_{D4},
observed mean d.c. input current. $I_{dc(AV)}$.

The curves of Figs. 8a to 8c are for the circuit configuration where the energy-recovery diodes D_3 and D_4 are tapped into the primary windings. Similar curves are obtained for the configuration where these diodes are connected to the ends of the windings and resistance is connected in series with these diodes. Three load conditions are shown: resistive loads of 20 and 47Ω, and no-load. All the curves show that the increase in current is a substantially linear function of supply voltage.

The current through diodes D_3 and D_4 can reach high values, with consequent high power dissipation in the resistances is series with the energy-recovery diodes when no tap is used. With a supply voltage of 250V and a resistive load of 20Ω, the mean total power dissipated in both resistances is approximately 160W. This method of energy absorption is therefore usually limited to input powers of 1kVA.

The turn-off time of the circuit t_{off} remains substantially constant over the supply voltage range.

Re-applied voltage

The anode-to-cathode voltage re-applied to the thyristor after commutation is shown in Fig. 9 for a range of supply voltage. Three load conditions are shown: resistive loads of 20 and 100Ω, and no-load; and the two circuit configurations: with and without diode taps.

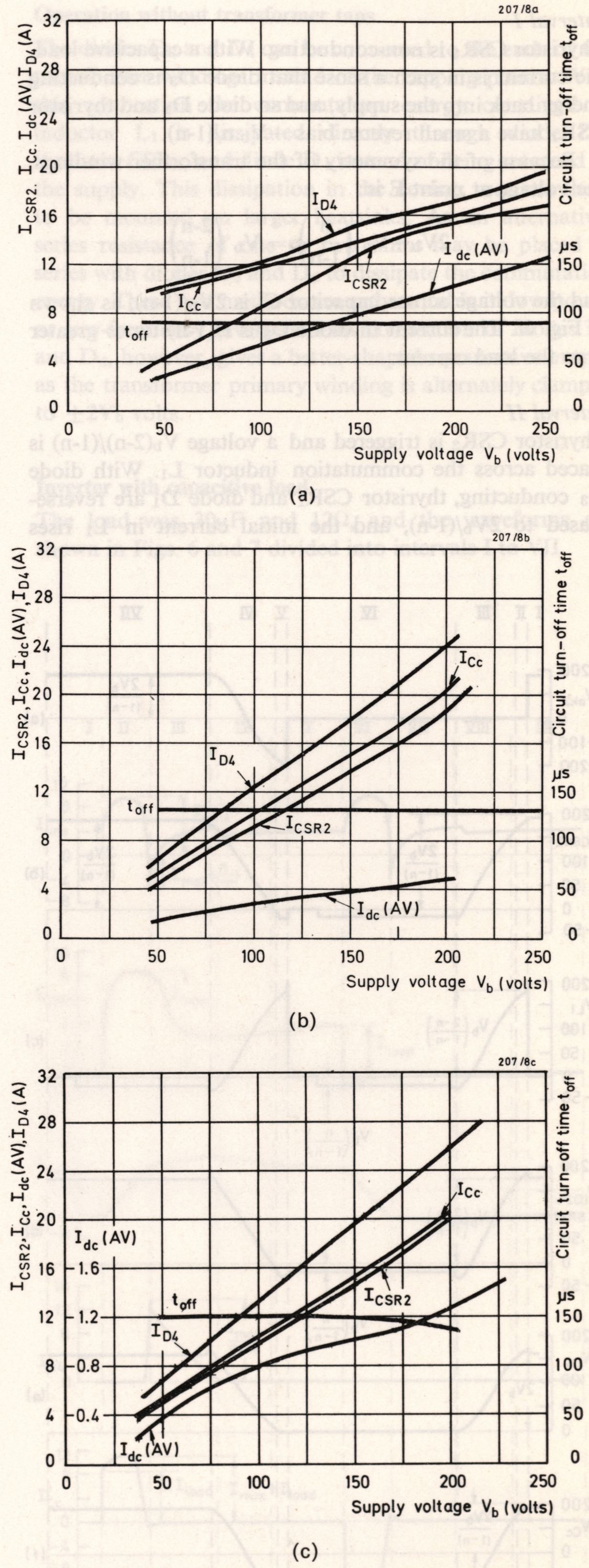

Fig. 8—Variation of thyristor, commutation capacitor, energy-recovery diode, and input currents, and commutation time, with supply voltage:
(a) resistive load 20Ω, n = 0·15
(b) resistive load 47Ω, n = 0·15
(c) resistive load ∞, n = 0·15

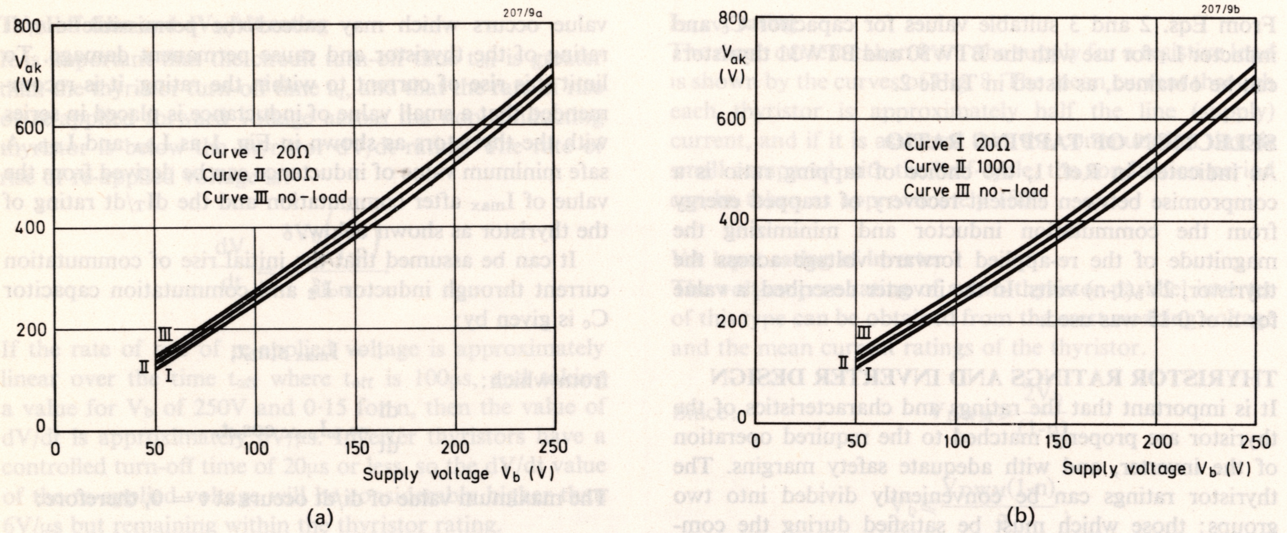

Fig. 9—Variation of re-applied thyristor voltage with supply voltage:
(a) resistive load, n = 0·15 (b) resistive load, n = 0, series resistance = 2·2Ω

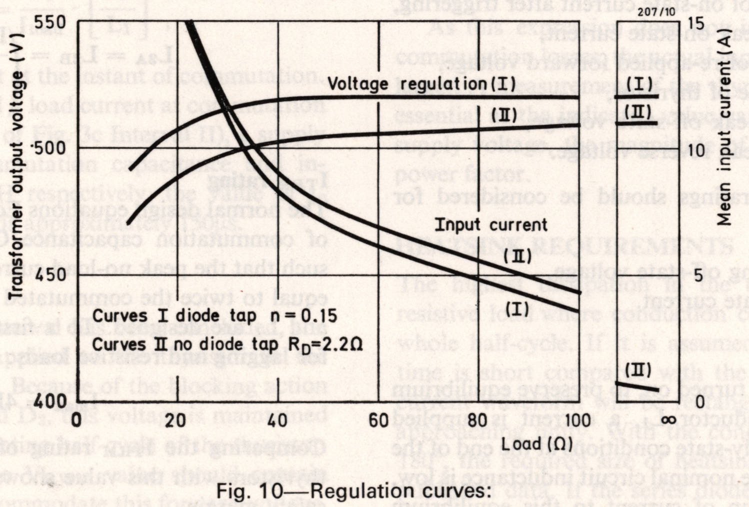

Fig. 10—Regulation curves:
variation of peak-to-peak output voltage and input current with resistive load

Regulation

Regulation curves for the inverter are shown in Fig. 10. The no-load to full-load regulation of the output voltage of the transformer secondary winding is about 12%. The d.c. input current is shown to be somewhat higher when diode dissipation resistances are used.

SELECTION OF COMMUTATION CAPACITOR AND INDUCTOR

The minimum values of commutation capacitance and inductance for impulse commutation of this type of inverter have been derived (Ref. 1). The values are given by the expressions:

$$C_{eff} = \frac{t_q\, I_{TO}}{0{\cdot}425 V_b}\,\mu F, \qquad \ldots(1)$$

$$L = \frac{t_q\, V_b}{0{\cdot}425 I_{TO}}\,\mu H, \qquad \ldots(2)$$

where t_q is the turn-off time of the thyristor for the load current prior to commutation (μs), I_{TO} is the current through the thyristor immediately before commutation (A), and V_b is the d.c. supply voltage (V).

The term C_{eff} is a function of the type of inverter and the position of the commutation capacitor. Eqs. 1 and 2 above refer to the half-bridge inverter where the capacitor is charged to the supply voltage V_b immediately before commutation. The blocking effect of diodes D_1 and D_2 results in the voltage across the capacitor being increased to $2V_b/1\text{-}n)$. Therefore to equate the same volt-ampere product to the capacitance, Eq. 1 has to be modified to:

$$C = \frac{t_q\, I_{TO}}{0{\cdot}425\left(\frac{2}{1\text{-}n}\right)^2 V_b}\,\mu F, \qquad \ldots(3)$$

From Eqs. 2 and 3 suitable values for capacitor C_c and inductor L_1 for use with the BTW30 and BTW31 thyristors can be obtained, as listed in Table 2.

SELECTION OF TAPPING RATIO

As indicated in Ref. 1, the choice of tapping ratio is a compromise between efficient recovery of trapped energy from the commutation inductor and minimizing the magnitude of the re-applied forward voltage across the thyristor, $2V_b(1\text{-}n)$ volts. In the inverter described, a value for n of 0·15 was used.

THYRISTOR RATINGS AND INVERTER DESIGN

It is important that the ratings and characteristics of the thyristor are properly matched to the required operation of the inverter, and with adequate safety margins. The thyristor ratings can be conveniently divided into two groups: those which must be satisfied during the commutation period, and those which must be satisfied during the steady-state conducting and non-conducting periods.

The following ratings should be considered during commutation:

dI_T/dt	rate of rise of on-state current after triggering,
I_{TRM}	repetitive peak on-state current,
dV_D/dt	rate of rise of re-applied forward voltage,
t_q	turn-off time of thyristor,
V_{DRM}	repetitive peak off-state voltage,
V_{RRM}	repetitive peak reverse voltage.

The following two ratings should be considered for steady-state operation:

V_{DWM}	crest working off-state voltage,
$I_{T(AV)}$	mean on-state current.

dI_T/dt rating

When thyristor CSR_2 is turned on, to preserve equilibrium in the commutation inductor L_1, a current is supplied equal to that in the steady-state conditions at the end of the preceding half-cycle. The nominal circuit inductance is low, so that a rapid build-up of current to this equilibrium value occurs which may exceed the permissible dI_T/dt rating of the thyristor and cause permanent damage. To limit this rise of current to within the rating, it is recommended that a small value of inductance is placed in series with the thyristors as shown in Fig. 1 as L_{2A} and L_{2B}. A safe minimum value of inductance can be derived from the value of I_{max} after commutation and the dI_T/dt rating of the thyristor as shown below.

It can be assumed that the initial rise of commutation current through inductor L_2 and commutation capacitor C_c is given by:

$$i = I_{max} \sin\omega t,$$

from which:

$$\frac{di}{dt} = \omega I_{max} \cos\omega t.$$

The maximum value of di/dt occurs at t = 0, therefore:

$$\left(\frac{di}{dt}\right)_{max} = \omega I_{max}.$$

Since:

$$\omega^2 = \frac{1}{L_2\, C_c},$$

$$L_{2A} = L_{2B} = \left(\frac{I_{max}}{\frac{di}{dt}}\right)^2 \cdot \frac{1}{C_c}. \qquad \ldots(4)$$

I_{TRM} rating

The normal design equations Eqs. 2 and 3 for the selection of commutation capacitance C_c and inductance L_1 are such that the peak no-load current through the thyristor is equal to twice the commutated load current for which C_c and L_1 are designed. To a first approximation, therefore, for lagging and resistive loads:

$$I_{max} = 4I_{T(AV)},$$

Comparing the I_{TRM} rating of the BTW30 and BTW31 thyristors with this value shows that there is an adequate safety margin.

TABLE 2

Commutation capacitance and inductance for inverters using BTW30 and BTW31 thyristors

$I_{T(AV)}$, squarewave d = 0·5	12	16	A
Thyristor turn-off time t_q at $I_{(AV)}$ above	300 to 600R: 10	300 to 600R: 25	μs
	800 to 1200R: 20	800 to 1200R: 35	μs
Minimum commutation capacitance	300 to 600R: 0·5 to 0·4	300 to 600R: 2·7 to 1·9	μF
	800 to 1200R: 1·2 to 0·3	800 to 1200R: 1·4 to 0·95	μF
Minimum commutation inductance	300 to 600R: 0·15 to 0·30	300 to 600R: 0·27 to 0·54	mH
	800 to 1200R: 0·8 to 1·2	800 to 1200R: 1·0 to 1·5	mH

Turn-off time and dV_D/dt rating

It is important that the circuit turn-off time t_{off} is greater than the thyristor turn-off time t_q, and that the rate of rise of re-applied forward voltage across the non-conducting thyristor is below the thyristor dV/dt rating. The rate of rise of re-applied voltage is:

$$\frac{dV}{dt} = \frac{\delta V_b\left(\frac{2}{1\text{-}n}\right)}{\delta t_{off}}.$$

If the rate of rise of re-applied voltage is approximately linear over the time t_{off} where t_{off} is 100μs, and taking a value for V_b of 250V and 0·15 for n, then the value of dV/dt is approximately 6V/μs. Inverter thyristors have a controlled turn-off time of 20μs or less, so the dV/dt value of the re-applied voltage will be considerably higher than 6V/μs but remaining within the thyristor rating.

The value of t_c, the time taken for the circuit to complete the commutation interval, is given by:

$$t_c = [L_1 C_{eff}]^{\frac{1}{2}} \tan^{-1} A \text{ seconds},$$

where:

$$A = \frac{V_b}{I_{load}} \cdot \left[\frac{C_{eff}}{L_1}\right]^{\frac{1}{2}},$$

and I_{load} is the load current at the instant of commutation. With an inductive load and a load current at commutation of 2A (as in the waveform of Fig. 3c Interval II), a supply voltage of 80V, and commutation capacitance and inductance of 2μF and 2mH respectively, the value of t_c from the above expression is approximately 150μs.

V_{DWM} rating

When the commutation interval has been concluded, the highest forward voltage applied to the thyristor in the blocking state is $2V_b/(1\text{-}n)$. Because of the blocking action of the series diodes D_1 and D_2, this voltage is maintained throughout the non-conducting half-cycle of the thyristor. As with V_{RRM} rating, the V_{DWM} value should contain an adequate margin to accommodate this forward voltage.

V_{DRM} rating

The required V_{DRM} rating of the thyristor will depend on the transients produced at the end of the commutation interval. Without suppression filters across the thyristors, an overshoot of approximately 20% immediately after commutation has been observed in this particular circuit. This overshoot appears to be caused by ringing of the dI/dt limiting inductor L_2 with the commutation capacitor when the series diode stops conducting. With adequate RC suppression filters across the thyristors and series diodes, the thyristor voltage waveform is largely free from transients.

V_{RRM} rating

The peak reverse voltage on the thyristor occurs when the commutation capacitor reverse-biases the thyristor, the maximum amplitude being $2V_b/(1\text{-}n)$. This value should be within the V_{RRM} rating of the thyristor.

$I_{T(AV)}$ rating

The mean current taken from the supply for a resistive load is shown by the curves of Fig. 8. The mean current through each thyristor is approximately half the line (supply) current, and if it is assumed that the commutation time is small compared with the half-cycle, the conduction period can be taken as approximately 180°.

VA input rating of inverter

The volt-ampere rating of a two-thyristor parallel inverter of this type can be obtained from the crest working voltage and the mean current ratings of the thyristor.

Since:

$$V_{DWM} \geqslant \frac{2V_b}{(1\text{-}n)}$$

$$V_b \leqslant \frac{V_{DWM}(1\text{-}n)}{2}.$$

The line current is approximately twice the $I_{T(AV)}$ rating, and so the volt-ampere rating based only on the thyristor parameters is:

$$VA \leqslant V_{DWM}\,(1\text{-}n)\, I_{T(AV)}.$$

As this expression does not include transformer and commutation losses, the actual input VA will be somewhat larger. A measurement of the thyristor off-state voltage is essential as the indicated value varies to some extent with supply voltage, the magnitude of the load, and the load power factor.

HEATSINK REQUIREMENTS

The highest dissipation in the thyristor occurs with a resistive load where conduction continues throughout the whole half-cycle. If it is assumed that the commutation time is short compared with the conduction period, the current waveform will be rectangular with a form factor approaching unity. With the conduction period taken as 180°, the required size of heatsink can be obtained from published data. If the series diodes D_1 and D_2 have stud-cathode connections, they can be mounted on the same heatsink as the corresponding thyristor.

For the energy-recovery diodes D_3 and D_4, it can be seen that the waveform over the conduction period can be approximately triangular with a peak value (for an inductive load) of $(I_{load}+I_{max})/(1\text{-}n)$ amperes. The mean current over one complete cycle is $\frac{1}{4}(I_{load}+I_{max})/(1\text{-}n)$ simplifying to a conduction period of 180°. The necessary heatsink size should be confirmed by checking the device mounting base temperature.

TRANSIENT SUPPRESSION

Normal transient suppression filters are required across each thyristor to limit the reverse voltage and current transients during the instant of commutation. These filters consist of a 220nF capacitor in series with 15Ω resistor across thyristors CSR_1 and CSR_2. Also, a 100nF capacitor and 15Ω resistor are connected across series diodes D_1 and D_2 to prevent overshoot at the end of the commutation waveform.

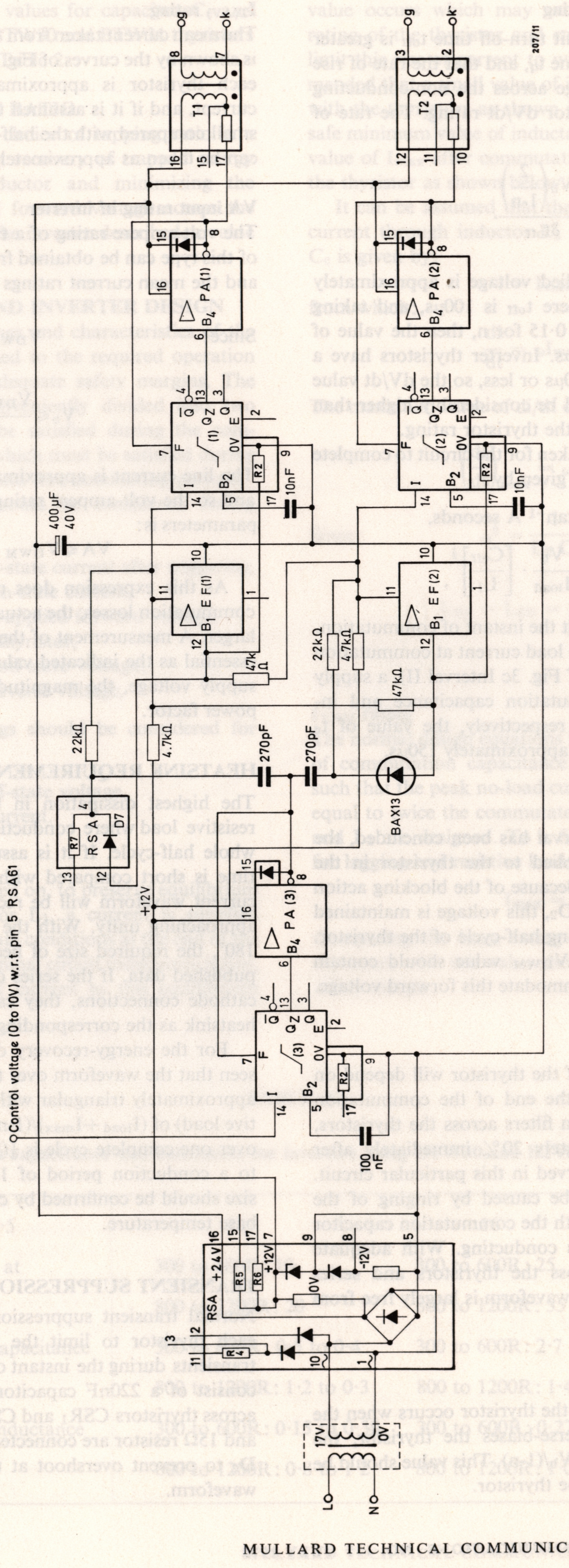
Control voltage (0 to 10V) w.r.t. pin 5 RSA61
400μF 40V
22kΩ
4.7kΩ
47kΩ
270pF
BAX13
10nF
100nF
+12V
+24V
12V
0V
RSA
R2
R4
R5
R6
R7
PA(1)
PA(2)
PA(3)
EF(1)
EF(2)
QZ
T1
17V
Lo
No
0k
0g
207/11

Fig. 11 Schematic circuit diagram of trigger system

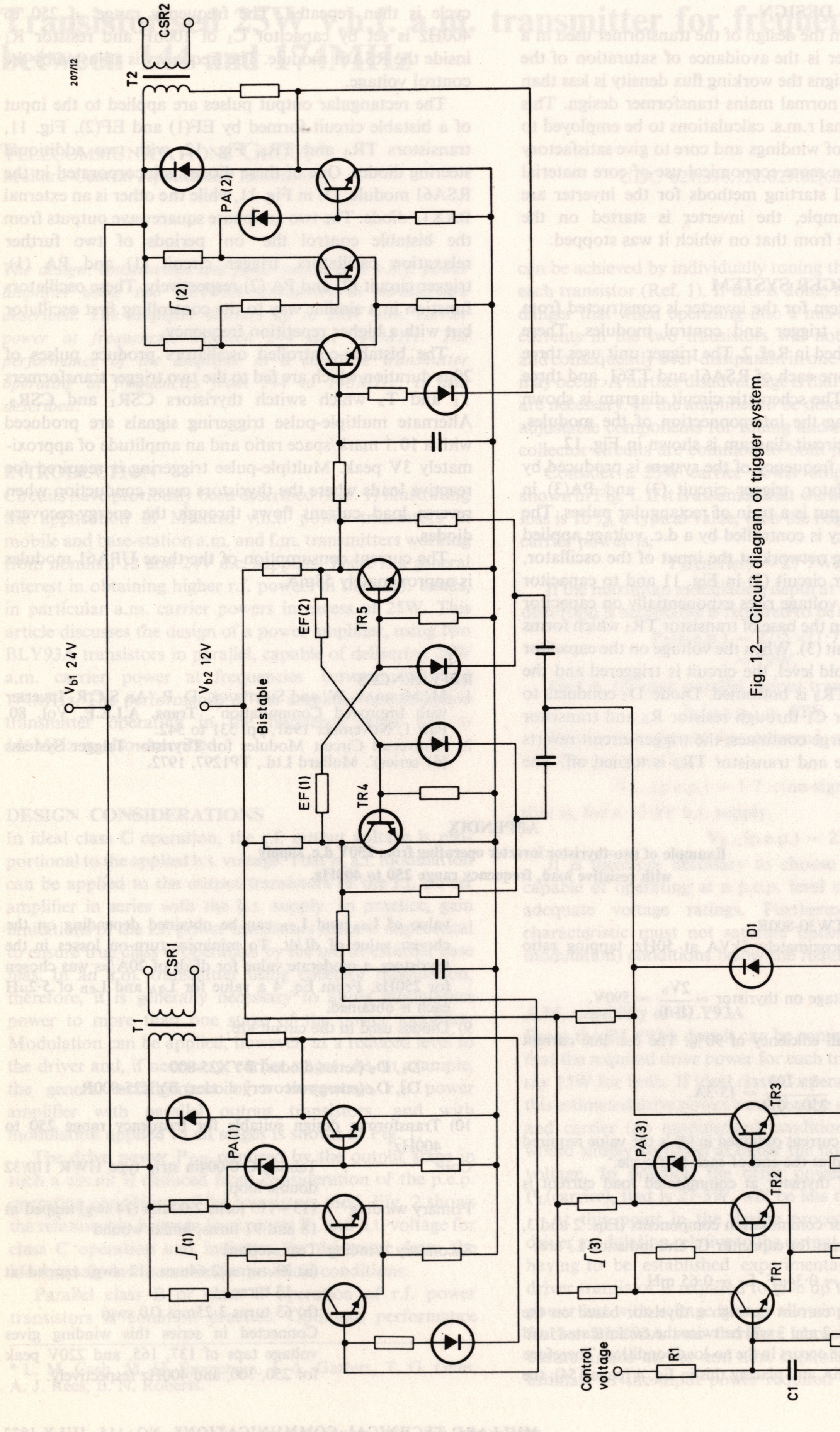
CSR2
T2
207/12
PA(2)
∫(2)
Vb1 24V
Vb2 12V
Bistable
EF(2)
TR5
EF(1)
TR4
CSR1
T1
PA(1)
∫(1)
D1
PA(3)
TR3
TR2
TR1
∫(3)
R1
R2
C1
Control voltage

Fig. 12 Circuit diagram of trigger system

TRANSFORMER DESIGN

A major criterion in the design of the transformer used in a squarewave inverter is the avoidance of saturation of the core. In simple designs the working flux density is less than half that used for normal mains transformer design. This value enables normal r.m.s. calculations to be employed to determine the size of windings and core to give satisfactory operation. Where a more economical use of core material is required, special starting methods for the inverter are required; for example, the inverter is started on the opposite half-cycle from that on which it was stopped.

INVERTER TRIGGER SYSTEM

The triggering system for the inverter is constructed from 61-series thyristor trigger and control modules. These modules are described in Ref. 2. The trigger unit uses three types of module, one each of RSA61 and TT61, and three UPA61 modules. The schematic circuit diagram is shown in Fig. 11, showing the interconnection of the modules, while the normal circuit diagram is shown in Fig. 12.

The controlling frequency of the system is produced by a relaxation oscillator, trigger circuit (3) and PA(3) in Fig. 11, whose output is a train of rectangular pulses. The repetition frequency is controlled by a d.c. voltage applied to the RC charging network at the input of the oscillator, to pin 14 of trigger circuit (3) in Fig. 11 and to capacitor C_1 in Fig. 12. The voltage rises exponentially on capacitor C_1, and therefore on the base of transistor TR_1 which forms part of trigger circuit (3). When the voltage on the capacitor reaches the threshold level, the circuit is triggered and the output transistor TR_3 is bottomed. Diode D_2 conducts to discharge capacitor C_1 through resistor R_2 and transistor TR_3. As the discharge continues, the trigger circuit reverts to its original state and transistor TR_3 is turned off. The cycle is then repeated. The frequency range of 250 to 400Hz is set by capacitor C_1 of 100nF and resistor R_1 inside the RSA61 module. The frequency is adjusted by the control voltage.

The rectangular output pulses are applied to the input of a bistable circuit formed by EF(1) and EF(2), Fig. 11, transistors TR_4 and TR_5, Fig. 12, with two additional steering diodes. One of these diodes is incorporated in the RSA61 module, D_7 in Fig. 11, while the other is an external BAX13 diode. The two antiphase squarewave outputs from the bistable control the 'on' periods of two further relaxation oscillators, trigger circuit (1) and PA (1), trigger circuit (2) and PA (2) respectively. These oscillators function in a similar way to the controlling first oscillator but with a higher repetition frequency.

The bistable-controlled oscillators produce pulses of 20μs duration which are fed to the two trigger transformers T_1 and T_2 which switch thyristors CSR_1 and CSR_2. Alternate multiple-pulse triggering signals are produced with a 10:1 mark/space ratio and an amplitude of approximately 3V peak. Multiple-pulse triggering is required for reactive loads where the thyristors cease conduction when reverse load current flows through the energy-recovery diodes.

The current consumption of the three UPA61 modules is approximately 58mA.

REFERENCES

1. McMurray, W. and Shattuck, D. P. 'An S.C.R. Inverter with Improved Commutation'. **Trans. A.I.E.E.** Vol. 80, Part 1, November 1961, pp. 531 to 542.
2. 'Universal Circuit Modules for Thyristor Trigger Systems (61 series)'. Mullard Ltd., TP1297, 1972.

APPENDIX

Example of two-thyristor inverter operating from 250V d.c. supply with resistive load, frequency range 250 to 400Hz.

1) Thyristor type BTW30-800R.
2) Transformer approximately 3kVA at 50Hz, tapping ratio $n = 0{\cdot}15$.
3) Peak forward voltage on thyristor $= \dfrac{2V_b}{(1\text{-}n)} = 590\text{V}$.
4) Assume an overall efficiency of 90%. The d.c. line current will be:

$$\frac{3\times10^3}{250\times0{\cdot}9} = 13{\cdot}3\text{A}.$$

5) The value of line current obtained in (4) is the value required to be commutated at the end of each half-cycle.
6) Turn-off time of thyristor at commutated load current is typically 15μs.
7) From equation for commutation components (Eqs. 2 and 3, page 153) the values for capacitor C_c and inductor L_1 are:

$$C_c = 0{\cdot}34\mu\text{F},\ L_1 = 0{\cdot}65\text{ mH}$$

8) The highest peak current through a thyristor based on the derivation of Eqs. 2 and 3 will be twice the commutated load current. This value occurs in the no-load condition. Therefore using a value 26·6A and placing this in Eq. 4 (page 154), the value of L_{2A} and L_{2B} can be obtained depending on the chosen value of dI/dt. To minimize turn-on losses in the thyristors, a moderate value for dI/dt of 20A/μs was chosen for 250Hz. From Eq. 4 a value for L_{2A} and L_{2B} of 5·2μH each is obtained.
9) Diodes used in the circuit are:

D_1, D_2 (series diodes) BYX25-800
D_3, D_4 (energy-recovery diodes) BYX25-800R

10) Transformer design suitable for frequency range 250 to 400Hz:

Core	Telmag C 0·004in strip type HWR 110/32 double loop
Primary winding	115+115 turns 2·00mm (14 swg) tapped at 18 and 97 turns, bifilar wound
Secondary Winding	Two sections (a) 39 turns 2·64mm (12 swg) tapped at 13 turns (b) 63 turns 3·25mm (10 swg) Connected in series this winding gives voltage taps of 137, 165, and 220V peak for 250, 300, and 400Hz respectively.

Transistorised 25W v.h.f. a.m. transmitter for frequencies between 144 and 174MHz

Telecommunications Group*
Mullard Central Application Laboratory

UDC 621.396.721.029.62[621.376.2]:621.375.4

The design, construction and performance of a v.h.f. power amplifier using two BLY93A transistors in parallel are described. The amplifier delivers up to 28W a.m. carrier power at frequencies between 144 and 174MHz. The performance of the amplifier in a complete transmitter operating at frequencies from 144 to 146MHz, is also described.

INTRODUCTION

Circuits have previously been described (Ref. 1) illustrating the application of Mullard v.h.f. power transistors in mobile and base-station a.m. and f.m. transmitters working from nominal 12 and 24V d.c. supplies. There is a general interest in obtaining higher r.f. powers in the v.h.f. bands, in particular a.m. carrier powers in excess of 25W. This article discusses the design of a power amplifier, using two BLY93A transistors in parallel, capable of delivering 28W a.m. carrier power at frequencies between 144 and 174MHz. The performance of the amplifier in a complete transmitter operating in the frequency range 144 to 146MHz is also described.

DESIGN CONSIDERATIONS

In ideal class C operation, the r.f. output voltage is proportional to the applied h.t. voltage. That is, a.f. modulation can be applied to the output transistors of the r.f. power amplifier in series with the h.t. supply. In practice, gain limitations of the r.f. power transistors make it unpractical to ensure true class C operation by the use of external base bias. In an a.m. transmitter using collector modulation, therefore, it is generally necessary to apply modulation power to more than one stage of the power amplifier. Modulation can be applied, however, at a reduced level to the driver and, if necessary, earlier stages. As an example, the general arrangement of a three-stage r.f. power amplifier with parallel output transistors, and with modulation applied to all stages is shown in Fig. 1.

The drive power P_{DR} required by the output stage in such a circuit is deduced from consideration of the p.e.p. operating conditions of the transistors used. Fig. 2 shows the relationship between load power P_L and h.t. voltage for class C operation and indicates the departure from the ideal square-law curve under practical conditions.

Parallel class B or class C operation of r.f. power transistors is common practice. Optimum performance can be achieved by individually tuning the input circuits of each transistor (Ref. 1). If this is done, however, there is a danger that when operating into a mis-matched load, the currents in the two transistors will not remain balanced and consequently over-dissipation in one or both transistors may occur. A further disadvantage is that extra components are necessary. In the amplifier to be described therefore, all adjustable components for tuning and matching base and collector circuits are common to both parallel transistors.

Consider a 25W carrier power amplifier arranged as shown in Fig. 1. If it is assumed that the aerial filter insertion loss is 10%, a typical value, then the required output stage carrier power is,

$$P_L(\text{carrier}) = 27{\cdot}5\text{W}.$$

If the maximum modulation depth at which the envelope distortion is acceptable is required to be 0·7 (or 70%), then,

$$\begin{aligned} P_L(\text{p.e.p.}) &= 27{\cdot}5\times(1{\cdot}7)^2, \\ &= 79\text{W}. \end{aligned}$$

That is, for each parallel output transistor,

$$P_L(\text{p.e.p.}) \simeq 40\text{W}.$$

This power should be delivered at an h.t. voltage $V_{\text{h.t.}}(\text{p.e.p.})$ given by,

$$V_{\text{h.t.}}(\text{p.e.p.}) = 1{\cdot}7\times(\text{no-signal h.t.}),$$

that is, for a 13·8V h.t. supply,

$$V_{\text{h.t.}}(\text{p.e.p.}) = 23{\cdot}4\text{V}.$$

It is therefore necessary to choose output transistors capable of operating at a p.e.p. level of about 40W with adequate voltage ratings. Furthermore, the P_L/P_{DR} characteristic must not saturate under dynamic (speech modulation) conditions below the required p.e.p. level.

A.M. capability of BLY93A

From the BLY93A data it can be conservatively estimated that the required drive power for each transistor is 7 to 8W, say 15W for both. If ideal class C operation were possible, this estimated drive power would be the same for both p.e.p. and carrier (no modulation) conditions, and the circuit would simply be tuned at either the nominal or p.e.p. h.t. voltage. In practice, the drive power required to give P_L(carrier), that is 27·5W, will be less than 15W.

At this point in the design procedure, the optimum driver modulation relative to the output stage is not known, having to be established experimentally. Therefore, the driver transistor is required to give up to 15W carrier load power but with voltage ratings allowing a.m. operation. A further BLY93A was therefore chosen as the driver to ensure ample carrier and a.m. capability. A conservative estimate of the input power required by the BLY93A is

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* L. M. Cash, M. H. Emmerson, J. A. Garters, T. G. Giles, A. J. Rees, B. N. Roberts.

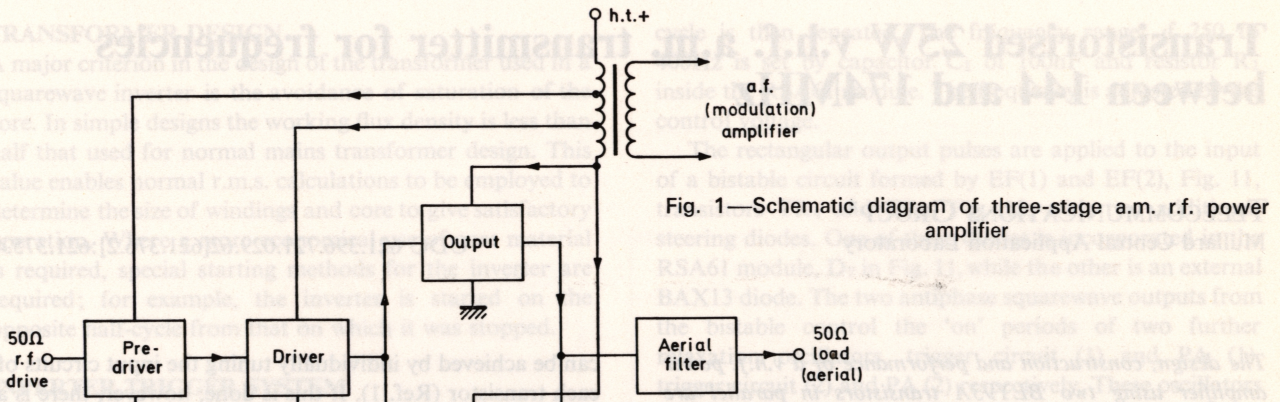
h.t.+
a.f. (modulation) amplifier
Output
Output
50Ω r.f. drive
Pre-driver
Driver
Aerial filter
50Ω load (aerial)

Fig. 1—Schematic diagram of three-stage a.m. r.f. power amplifier

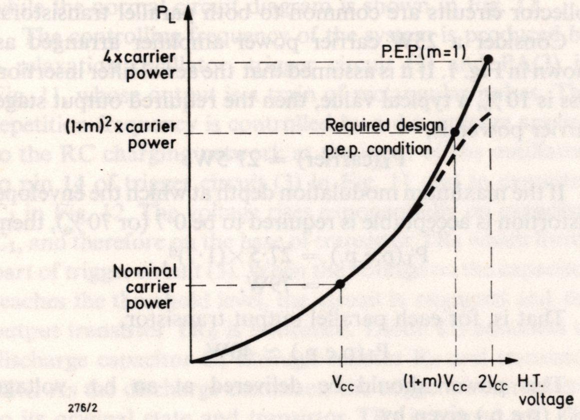

Fig. 2—Class C operation with collector modulation. Full curve represents ideal class C operation, and dotted curve is for practical conditions

4W. This can be obtained from a BLY97 pre-driver transistor which is capable of delivering 4W load power at 13·8V for a drive power of less than 0·3W with a.m. capability.

R.F. POWER AMPLIFIER DESIGN AND C.W. MEASUREMENTS

The circuit diagram of the power amplifier is shown in Fig. 3. Conventional circuit design practice is followed except that initially the 13·8V h.t. was supplied to the parallel output transistors via separate decoupling components, with ceramic blocking capacitors C_{17} and C_{18} in the collector circuits to facilitate observation of the individual collector currents with mismatched loads. This feature was omitted in later versions of the circuit when current sharing had been measured.

The printed circuit board layout is shown in Fig. 4. The board is $\frac{3}{32}$" resin-bonded glass fibre, double-clad with 2oz./sq.ft. (0·07mm) copper. A continuous earth plane is obtained by edge-plating the board and through-hole plating the transistor clearance holes. The through-hole plating needs to be removed in the region of the collector and base islands; an alternative is to remove a 1mm strip from the collector and base islands adjacent to the holes. The board is designed so that the area of free ground plane near the driver and output transistors is sufficient to conduct heat away from the devices. If this is not done, ferrite-cored components such as L_9 and L_{10} may overheat.

C.W. measurements at 174MHz

For extended r.f. measurements under laboratory conditions, the power amplifier printed circuit board was mounted on a block of black anodised aluminium, dimensions 126×81×12mm. Retaining nuts were used to pull each transistor mounting base into good thermal contact with the surface of the block. The block and printed circuit board were bolted onto a 127mm length of black anodised extruded aluminium heatsink, type 60D.

The amplifier was first tuned for c.w. operation into a 50Ω load at 174MHz, with the h.t. at 13·8V and P_{DR} at 300mW. The initial measurements are given in Table 1.

TABLE 1

Collector currents at f = 174MHz, h.t. = 13·8V, and P_{DR} = 300mW

Pre-driver (BLY97) collector current, I_{C1}		400mA
Driver (BLY93A) collector current, I_{C2}		2·1A
Output stage (BLY93A) collector currents,	I_{C3}	2·65A
	I_{C4}	2·75A
Load power, P_L		49W

These results indicate that there is sufficient excess power capability to allow tuning for a.m. operation at 27·5W load carrier power.

The current sharing of the output transistors with the amplifier operating into mismatched loads was measured. The simultaneous maximum values of I_{C3} and I_{C4} were measured for various load impedance phase angles (Table 2).

TABLE 2

Output stage collector currents for different load v.s.w.r. values at f = 174MHz, h.t. = 13·8V, and P_{DR} = 300mW

Load v.s.w.r.	P_L (incident) (W)	P_L (reflected) (W)	I_{C3} max (A)	I_{C4} max (A)
1	49	0	2·65	2·75
3	32	7·5	3·4	3·5
10	35	20	4·05	3·95

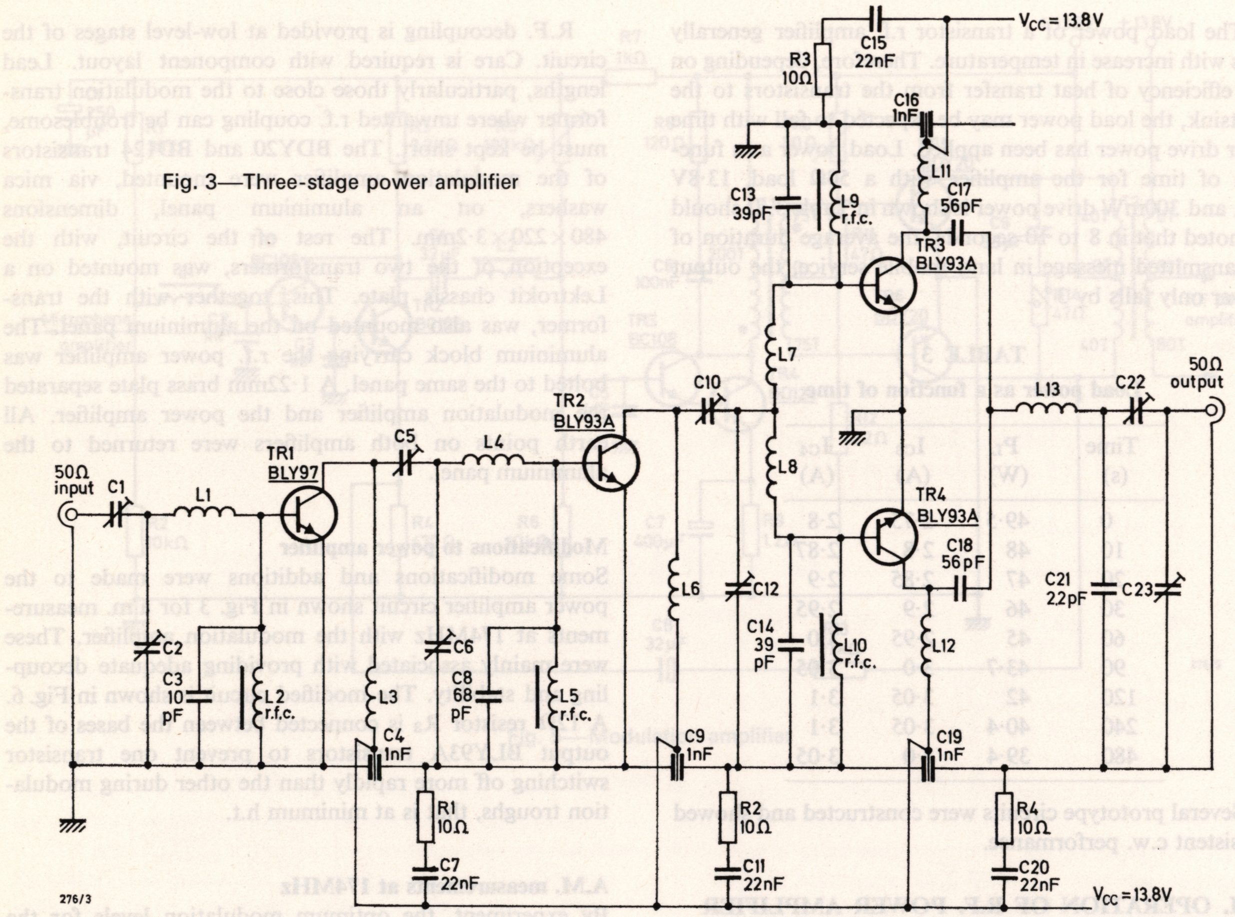
VCC=13·8V
C15 22nF
R3 10Ω
C16 1nF
L11
C17 56pF
C13 39pF
L9 r.f.c.
TR3 BLY93A
L7
C10
L8
TR2 BLY93A
C5
L4
TR1 BLY97
50Ω input
C1
L1
C2
C3 10 pF
L3
L2 r.f.c.
C6
C8 68 pF
L5 r.f.c.
C4 1nF
L6
C12
C14 39 pF
L10 r.f.c.
TR4 BLY93A
C18 56pF
L12
C9 1nF
C19 1nF
L13
C22
C21 2.2pF
C23
50Ω output
R1 10Ω
C7 22nF
R2 10Ω
C11 22nF
R4 10Ω
C20 22nF
VCC=13·8V
276/3

Fig. 3—Three-stage power amplifier

Coil data

No.	Turns	En cu diam. (mm)	Internal diam. (mm)	Length (mm)
L_1, L_4	2	1·25	7	8
L_3, L_6	4	1·25	7	8
L_7, L_8	2	1·25	5	7
L_{11}, L_{12}	3	1·25	7	7
L_{13}	2	1·60	7	5
L_2	2 turns, 0·46mm enamelled copper wire wound on an FX1115 Ferroxcube bead			
L_5, L_9, L_{10}	2·5 turns, 0·5mm tinned copper wire wound on FX1898 Ferroxcube bead			

Resistors

All resistors are carbon film, style CR37.

Capacitors

Trimmer capacitors are all 4 to 40pF, Mullard type 809 08002. Capacitors C_7, C_{11} and C_{20} are 22nF, Mullard type C280AE/P22K. All others except for feed-through capacitors are ceramic tubular.

Transistors

TR_1	BLY97
TR_2, TR_3, TR_4	BLY93A

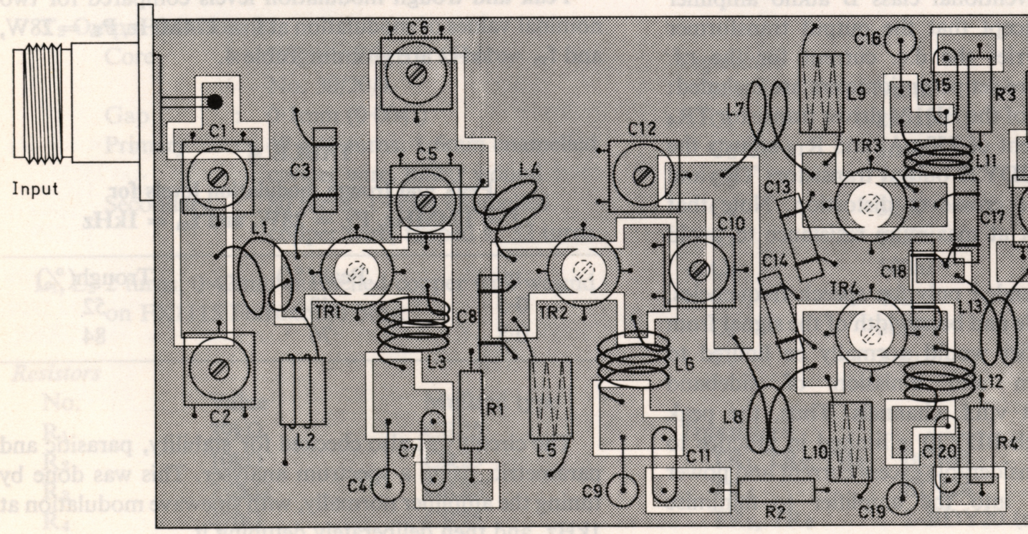
Input
Output
C6
C1
C3
C5
C12
L4
L7
L9
C16
C15
R3
C23
TR3
L11
C13
C10
C17
C22
L1
TR1
C8
TR2
C14
TR4
C18
L13
L3
L6
C21
C2
L2
R1
L5
L8
L10
C20
L12
R4
C7
C4
C9
C11
R2
C19
276/4

Fig. 4—Layout of printed circuit board

The load power of a transistor r.f. amplifier generally falls with increase in temperature. Therefore, depending on the efficiency of heat transfer from the transistors to the heatsink, the load power may be expected to fall with time after drive power has been applied. Load power as a function of time for the amplifier with a 50Ω load, 13·8V h.t., and 300mW drive power is shown in Table 3. It should be noted that in 8 to 10 seconds, the average duration of a transmitted message in land mobile service, the output power only falls by 3%.

TABLE 3

Load power as a function of time

Time (s)	P_L (W)	I_{C3} (A)	I_{C4} (A)
0	49·5	2·75	2·8
10	48	2·8	2·87
20	47	2·85	2·9
30	46	2·9	2·95
60	45	2·95	3·0
90	43·7	3·0	3·05
120	42	3·05	3·1
240	40·4	3·05	3·1
480	39·4	3·0	3·05

Several prototype circuits were constructed and showed consistent c.w. performance.

A.M. OPERATION OF R.F. POWER AMPLIFIER

For assessment of the a.m. performance of the amplifier, an r.f. driver and a modulation amplifier were required.

R.F. driver

The r.f. driver circuit used has been described in a previous publication (Ref. 1). Although designed for operation in the band 156 to 174MHz, this circuit can in fact be tuned to frequencies below 156MHz.

Modulation amplifier

A modulation amplifier capable of supplying over 15W is shown in Fig. 5. Conventional class B audio amplifier practice is followed except that the output transformer secondary winding carries the d.c. current for the r.f. power amplifier. Two pre-set potentiometers are included: R_5 sets the class A bias of the BD124 driver transistor TR_4 to give a collector current of 750mA, and R_{10} adjusts the bias of the matched 2-BDY20 output transistors TR_5 and TR_6 to give acceptable crossover distortion. Note that initially R_5 must be set at maximum resistance to avoid over dissipation in TR_4.

The amplifier is intended only for speech frequencies, and in fact the amplitude and bandwidth of the signal from the microphone amplifier would normally be limited to avoid over-modulation and emission of sideband frequencies in adjacent v.h.f. channels. Thus, the peak collector current in each BDY20 is limited in practice to about 2A. However, considerable excess current and power capability is designed into the amplifier to minimise distortion.

R.F. decoupling is provided at low-level stages of the circuit. Care is required with component layout. Lead lengths, particularly those close to the modulation transformer where unwanted r.f. coupling can be troublesome, must be kept short. The BDY20 and BD124 transistors of the modulation amplifier were mounted, via mica washers, on an aluminium panel, dimensions 480×220×3·2mm. The rest of the circuit, with the exception of the two transformers, was mounted on a Lektrokit chassis plate. This, together with the transformer, was also mounted on the aluminium panel. The aluminium block carrying the r.f. power amplifier was bolted to the same panel. A 1·22mm brass plate separated the modulation amplifier and the power amplifier. All earth points on both amplifiers were returned to the aluminium panel.

Modifications to power amplifier

Some modifications and additions were made to the power amplifier circuit shown in Fig. 3 for a.m. measurements at 174MHz with the modulation amplifier. These were mainly associated with providing adequate decoupling and stability. The modified circuit is shown in Fig. 6. A 12Ω resistor R_3 is connected between the bases of the output BLY93A transistors to prevent one transistor switching off more rapidly than the other during modulation troughs, that is at minimum h.t.

A.M. measurements at 174MHz

By experiment, the optimum modulation levels for the driver and pre-driver stages were found both to be 40% of the output stage level; the modulation transformer was tapped at 32 turns, as shown.

Tuning was performed by minimising the modulation envelope distortion, observed on an oscilloscope, and by comparing peak and trough modulation levels measured on a modulation meter (Marconi TF2300). It was found that the distortion present was substantially that of the modulation amplifier, caused by the non-linear impedance offered by the power amplifier. This could be reduced by resistively loading the modulation transformer secondary.

Peak and trough modulation levels compared for two nominal values of modulation at $f = 174\text{MHz}$, $P_L = 28\text{W}$, and $f_m = 1\text{kHz}$ are given in Table 4.

TABLE 4

Peak and trough modulation levels for $f = 174\text{MHz}$, $P_L = 28\text{W}$, and $f_m = 1\text{kHz}$

m	Peak(%)	Trough(%)
0·5	48	52
0·8	76	84

The circuit was also checked for stability, parasitic and parametric, using a spectrum analyser. This was done by tuning the amplifier normally, with sinewave modulation at 1kHz, and then deliberately detuning it.

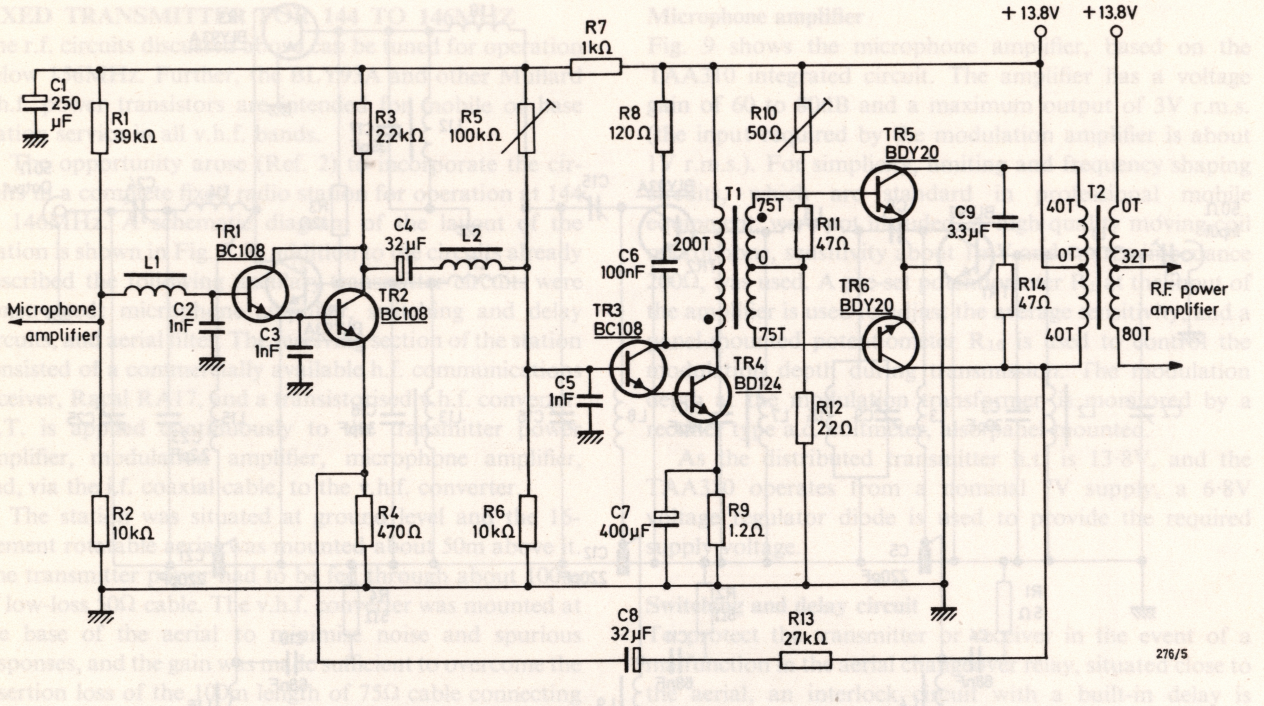

Fig. 5—Modulation amplifier

Transformer and choke data

T_1 Driver transformer

Core : Unisil 51 (Grain-orientated silicon iron)
Gap : 0·127mm (0·005″)
Primary : 200 turns, 0·56mm (24 s.w.g.) enamelled copper wire
Secondary : 75+75 turns, 0·38mm (28 s.w.g.) enamelled copper wire, bifilar wound

T_2 Output transformer

Core : English Electric C-core, No. 30/20/4
Gap : 0·1mm (0·004″)
Primary : 40+40 turns, 1·6mm enamelled copper wire, bifilar wound
Secondary : 80 turns, 1·6mm enamelled copper wire, tapped at 32 turns

L_1, L_2 2 turns, 0·42mm enamelled copper wire wound on FX1115 Ferroxcube bead

Resistors

No.	Value	Mullard type
R_1	39kΩ	CR25
R_2	10kΩ	CR25
R_3	2·2kΩ	CR25
R_4	470Ω	CR25
R_5	100kΩ	
R_6	10kΩ	CR25
R_7	1kΩ	CR25
R_8	120Ω	CR37
R_9	1·2Ω 3W w.w.	
R_{10}	50Ω	
R_{11}	47Ω 8W w.w.	
R_{12}	2·2Ω	CR37
R_{13}	27kΩ	CR37
R_{14}	47Ω 8W w.w.	

Capacitors

No.	Value	Mullard type
C_1	250μF	C437/E250
C_2	1nF	425 21002
C_3	1nF	425 21002
C_4	32μF	C428AR/E32
C_5	1nF	425 21002
C_6	100nF	344 21104
C_7	400μF	C437/D400
C_8	32μF	C428AR/E32
C_9	3·3μF	344 21335

Transistors

TR_1, TR_2, TR_3	BC108
TR_4	BD124
TR_5, TR_6	2–BDY20 (matched)

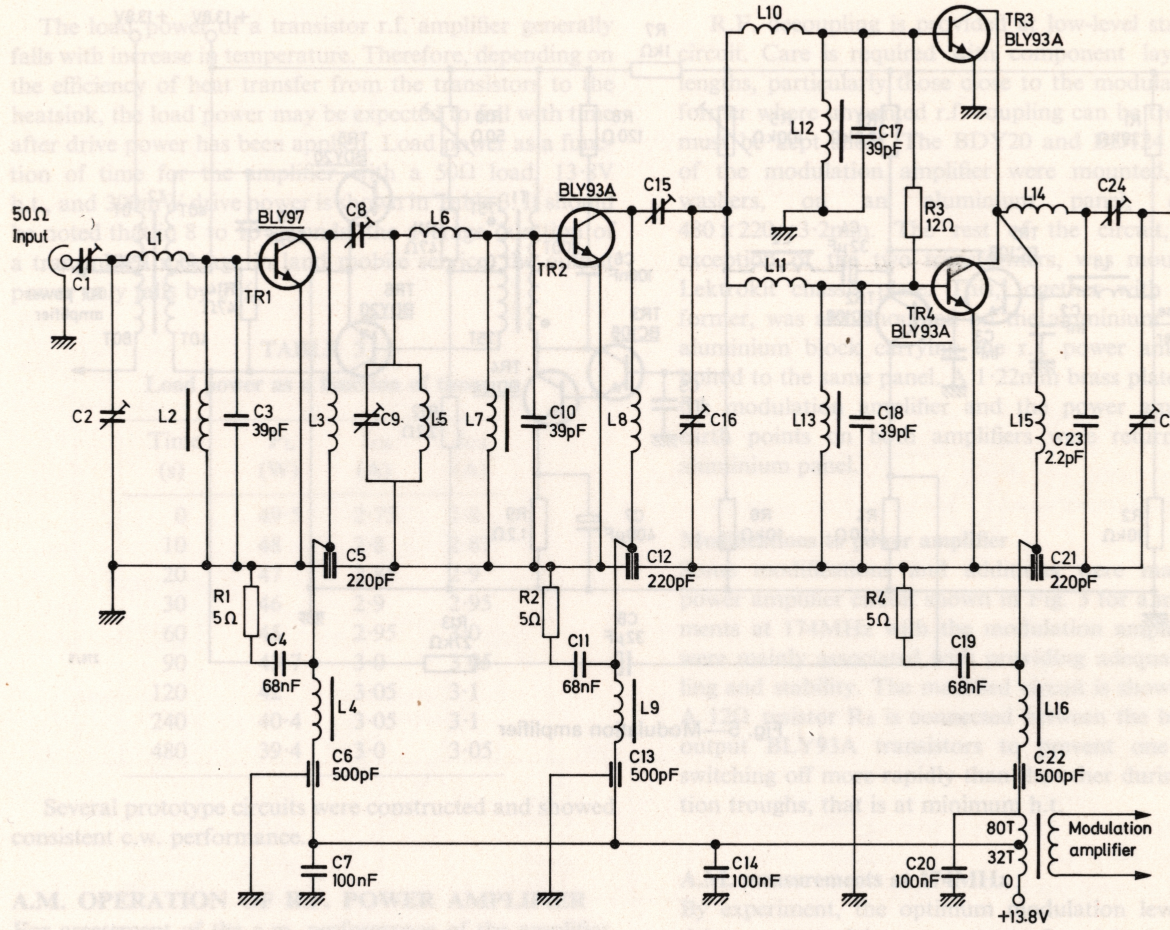
50Ω Input
C1
L1
BLY97
TR1
C8
L6
BLY93A
TR2
C15
L10
TR3 BLY93A
L12
C17 39pF
R3 12Ω
L14
C24
50Ω Output
L11
TR4 BLY93A
C2
L2
C3 39pF
L3
C9
L5
L7
C10 39pF
L8
C16
L13
C18 39pF
L15
C23 2.2pF
C25
C5 220pF
C12 220pF
C21 220pF
R1 5Ω
R2 5Ω
R4 5Ω
C4 68nF
C11 68nF
C19 68nF
L4
L9
L16
C6 500pF
C13 500pF
C22 500pF
80T
32T
Modulation amplifier
C7 100nF
C14 100nF
C20 100nF
+13.8V
276/6

Fig. 6—Modified three-stage power amplifier for a.m. operation

Coil data

	Turns	En. cu diameter (mm)	Internal diameter (mm)	Length (mm)
L_1	2	1·25	5	9
L_3, L_8, L_{15}	3	1·25	6·3	9
L_5	2	1·25	8·3	5
L_6	2	1·25	6·3	8
L_{10}, L_{11}	2	1·25	6	8
L_{14}	2	1·60	8·5	6·5 (10mm including end leads)

L_2	2·5 turns, 0·40mm enamelled copper wire wound on FX1115 Ferroxcube bead
L_4, L_9, L_{16}	2·5 turns, 0·5mm tinned copper wire wound on FX1898 Ferroxcube bead
L_7	1·5 turns, 0·40mm enamelled copper wire wound on FX1115 Ferroxcube bead
L_{12}, L_{13}	1·5 turns, 0·5mm tinned copper wire wound on FX1898 Ferroxcube bead

Resistors

All resistors are carbon film, style CR37, except for R_3 which is 12Ω, 0·5W metal oxide Electrosil, type TR5.

Capacitors

Trimmer capacitors are all 4 to 40pF, Mullard type 809 08002. Capacitors C_4, C_{11} and C_{19} are 68nF, Mullard type C280/P68K. Capacitors C_7, C_{14}, and C_{20} are 100nF, Mullard type C280/P100K. All others except for feed-through and stand-off capacitors are ceramic tubular.

Transistors

TR_1	BLY97
TR_2, TR_3, TR_4	BLY93A

FIXED TRANSMITTER FOR 144 TO 146MHZ

The r.f. circuits discussed above can be tuned for operation below 156MHz. Further, the BLY93A and other Mullard v.h.f. power transistors are intended for mobile or base station service in all v.h.f. bands.

The opportunity arose (Ref. 2) to incorporate the circuits in a complete fixed radio station for operation at 144 to 146MHz. A schematic diagram of the layout of the station is shown in Fig. 7. In addition to the circuits already described the following ancillary transmitter circuits were constructed: microphone amplifier, switching and delay circuits, and aerial filter. The receiving section of the station consisted of a commercially available h.f. communications receiver, Racal RA17, and a transistorised v.h.f. converter. H.T. is applied continuously to the transmitter power amplifier, modulation amplifier, microphone amplifier, and, via the i.f. coaxial cable, to the v.h.f. converter.

The station was situated at ground level and the 16-element rotatable aerial was mounted about 50m above it. The transmitter power had to be fed through about 100m of low-loss 50Ω cable. The v.h.f. converter was mounted at the base of the aerial to minimise noise and spurious responses, and the gain was made sufficient to overcome the insertion loss of the 100m length of 75Ω cable connecting the converter to the receiver.

A remotely controlled coaxial transmit/receive switch operating at 18V was mounted close to the aerial. The aerial rotation mechanism was also remotely controlled.

The layout of the transmitter circuits is shown in Fig. 8. Provision was made for operation in three channels by including three switched v.h.f. driver circuits, crystal controlled at 145·0500MHz, 144·8090MHz, and 144·6605 MHz.

Microphone amplifier

Fig. 9 shows the microphone amplifier, based on the TAA310 integrated circuit. The amplifier has a voltage gain of 60 to 80dB and a maximum output of 3V r.m.s. (the input required by the modulation amplifier is about 1V r.m.s.). For simplicity, limiting and frequency shaping circuits, which are standard in professional mobile equipment, were not included. A high quality moving-coil microphone, sensitivity about 1mV and source impedance 200Ω, was used. A pre-set potentiometer R_1 at the input of the amplifier is used to adjust the average sensitivity, and a panel-mounted potentiometer R_{10} is used to control the modulation depth during transmission. The modulation depth at the modulation transformer is monitored by a rectifier type a.c. voltmeter, also panel-mounted.

As the distributed transmitter h.t. is 13·8V, and the TAA310 operates from a nominal 7V supply, a 6·8V voltage regulator diode is used to provide the required supply voltage.

Switching and delay circuit

To protect the transmitter or receiver in the event of a malfunction in the aerial changeover relay, situated close to the aerial, an interlock circuit with a built-in delay is included in the system. The circuit is shown in Fig. 10.

The changeover relay is in the 'receive' position when not energised. The sequence of events on selecting 'transmit' is as follows.

1) After a brief delay (<1ms), set by capacitor C_1, the BCY38 transistor TR_1 turns on and the changeover relay is activated. The energising current is 45mA.
2) After a longer delay (about 200ms) set by capacitor C_2, the second BCY38 transistor TR_2 turns on and switches

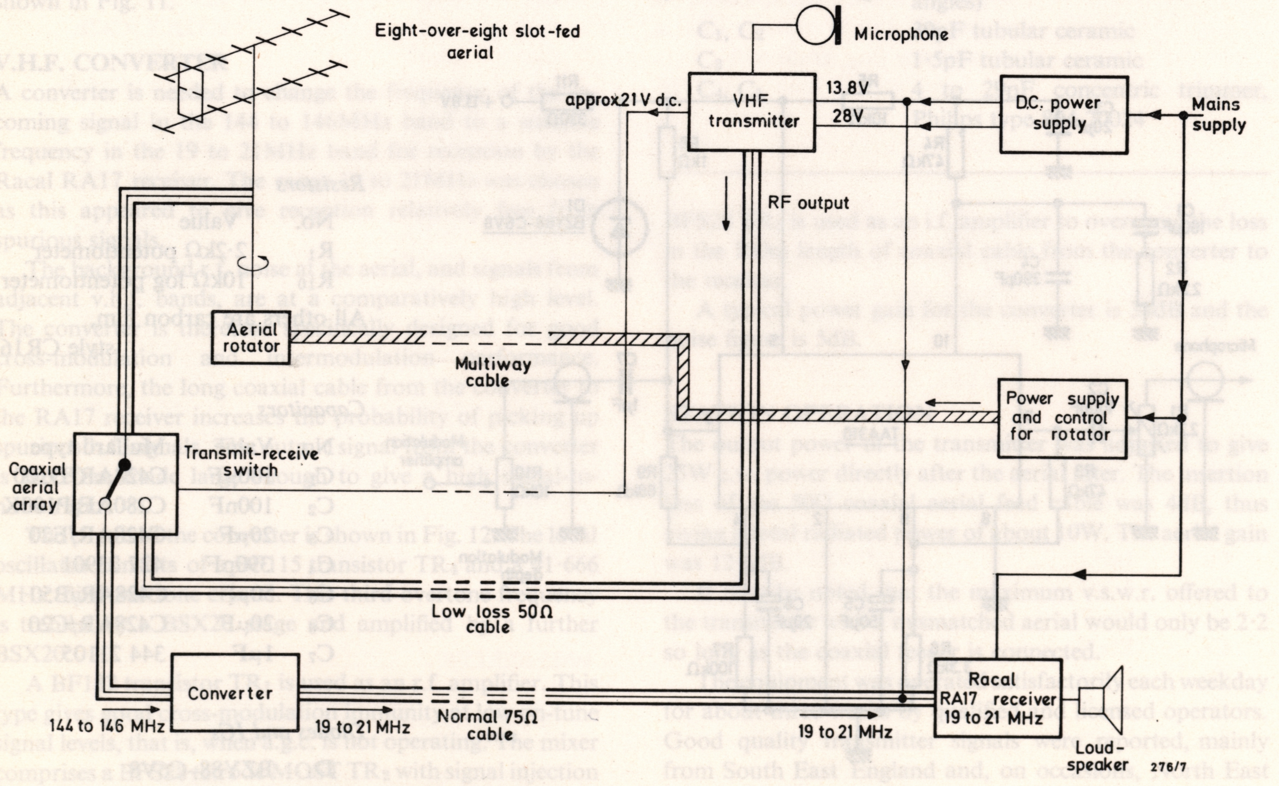
Eight-over-eight slot-fed aerial
Microphone
approx 21V d.c.
VHF transmitter
13.8V
28V
D.C. power supply
Mains supply
RF output
Aerial rotator
Multiway cable
Power supply and control for rotator
Coaxial aerial array
Transmit-receive switch
Low loss 50Ω cable
Converter
144 to 146 MHz
19 to 21 MHz
Normal 75Ω cable
19 to 21 MHz
Racal RA17 receiver 19 to 21 MHz
Loud-speaker
276/7

Fig. 7—Schematic diagram of 144 to 146MHz fixed station

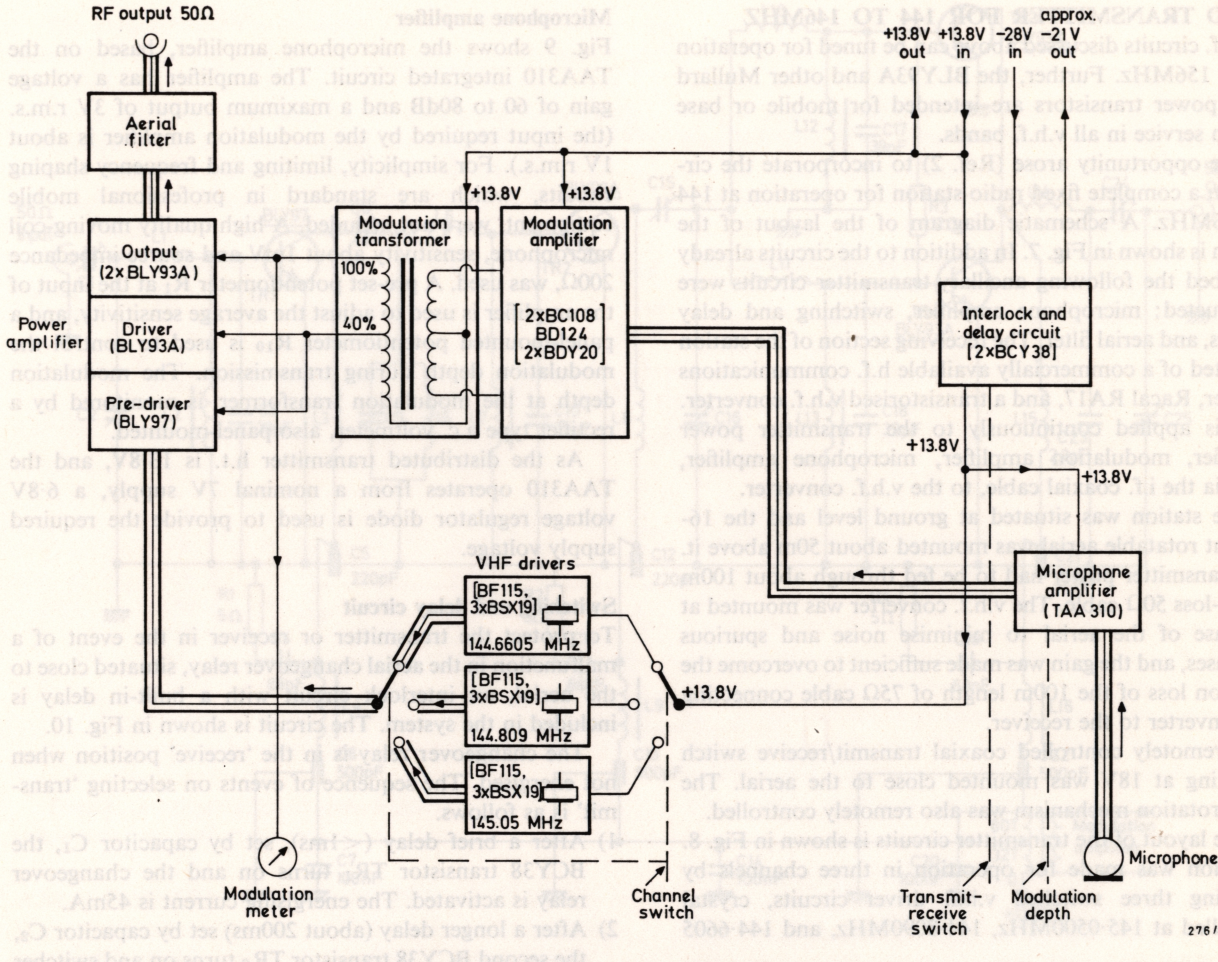
RF output 50Ω
Aerial filter
+13.8V
+13.8V
Output (2×BLY93A)
Power amplifier
Driver (BLY93A)
Pre-driver (BLY97)
Modulation transformer
100%
40%
Modulation amplifier
2×BC108
BD124
2×BDY20
+13.8V out
+13.8V in
−28V in
approx. −21V out
Interlock and delay circuit [2×BCY38]
+13.8V
+13.8V
Microphone amplifier (TAA 310)
VHF drivers
[BF115, 3xBSX19]
144.6605 MHz
[BF115, 3xBSX19]
144.809 MHz
[BF115, 3xBSX19]
145.05 MHz
+13.8V
Microphone
Modulation meter
Channel switch
Transmit-receive switch
Modulation depth
276/8/4

Fig. 8—Schematic diagram of 25W a.m. transmitter

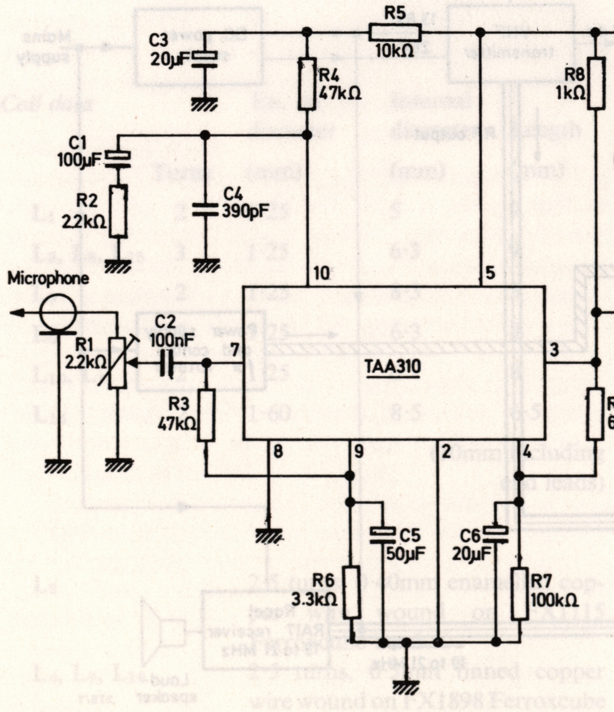
C3
20µF
R5
10kΩ
R11
330Ω
+13.8V
R4
47kΩ
R8
1kΩ
C1
100µF
R2
2.2kΩ
C4
390pF
D1
BZY88-C6V8
Microphone
R1
2.2kΩ
C2
100nF
R3
47kΩ
TAA310
10
5
7
3
8
9
2
4
C7
1µF
Modulation amplifier
R10
10kΩ
R9
68kΩ
Modulation depth
C5
50µF
C6
20µF
R6
3.3kΩ
R7
100kΩ
276/9

Fig. 9—Microphone amplifier

Resistors

No.	Value
R_1	2·2kΩ potentiometer
R_{10}	10kΩ log potentiometer

All others are carbon film, style CR16

Capacitors

No.	Value	Mullard type
C_1	100µF	C428AR/D100
C_2	100nF	C280AE/P100K
C_3	20µF	C428AR/E20
C_4	390pF	427 23901
C_5	50µF	C428AR/B50
C_6	20µF	C428AR/C20
C_7	1µF	344 21105

Diodes and ICs

D_1	BZY88–C6V8
IC	TAA310

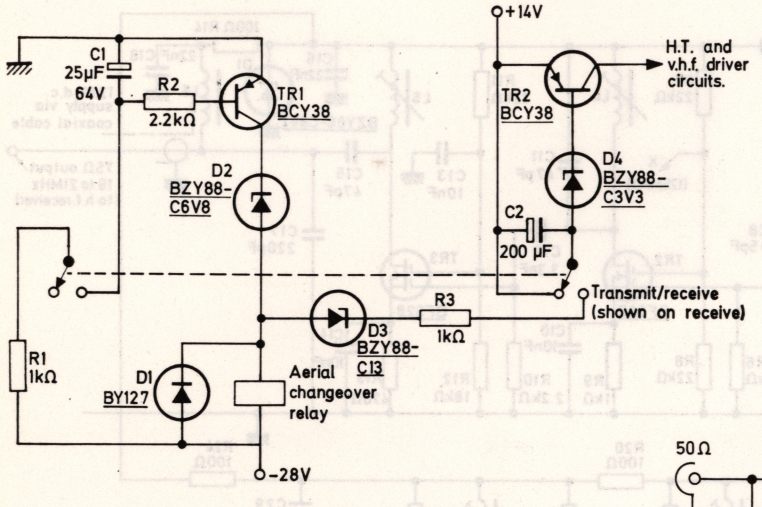
+14V
C1
25µF
64V
R2
2.2kΩ
TR1
BCY38
TR2
BCY38
H.T. and v.h.f. driver circuits.
D2
BZY88-C6V8
D4
BZY88-C3V3
C2
200µF
Transmit/receive (shown on receive)
R3
1kΩ
D3
BZY88-C13
R1
1kΩ
D1
BY127
Aerial changeover relay
−28V

Fig. 10—Switching and delay circuit

Resistors
All resistors are CR37 style.

Capacitors

No.	Value	Mullard type
C_1	25µF	C428AR/G25
C_2	200µF	C428AR/D200

Diodes and transistors

D_1	BY127
D_2	BZY88–C6V8
D_3	BZY88–C13
D_4	BZY88–C3V3
TR_1, TR_2	BCY38

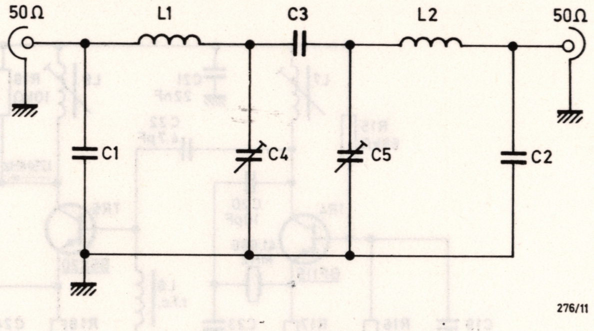
50Ω
L1
C3
L2
50Ω
C1
C4
C5
C2
276/11

Fig. 11—Transmitter aerial filter

L_1, L_2	5·5 turns, 1·25mm enamelled copper wire, internal diameter 6mm, length 9mm (mounted mutually at right-angles)
C_1, C_2	39pF tubular ceramic
C_3	1·5pF tubular ceramic
C_4, C_5	4 to 29pF concentric trimmer, Philips type 804 20024

h.t. to the selected v.h.f. drive circuit. This does not take place unless an h.t. voltage of −28V is present on the relay, and the relay winding is intact.

On switching to 'receive', capacitor C_2 discharges very rapidly, switching off TR_2 and the supply to the v.h.f. driver, and after about 150ms, set by C_1, TR_1 turns off and the relay returns to the receive position.

Because h.t. is applied continuously to the v.h.f. converter, it was necessary when on 'transmit' to reduce receiver noise using the 'mute' control of the RA17 receiver.

Aerial filter

The aerial filter is of the conventional bandpass type and is shown in Fig. 11.

V.H.F. CONVERTER

A converter is needed to change the frequency of the incoming signal in the 144 to 146MHz band to a suitable frequency in the 19 to 21MHz band for reception by the Racal RA17 receiver. The range 19 to 21MHz was chosen as this appeared to give reception relatively free from spurious signals.

The background r.f. noise at the aerial, and signals from adjacent v.h.f. bands, are at a comparatively high level. The converter is therefore specifically designed for good cross-modulation and intermodulation performance. Furthermore, the long coaxial cable from the converter to the RA17 receiver increases the probability of picking up spurious h.f. signals. The output signal from the converter is therefore made large enough to give a high signal-to-noise ratio.

The circuit of the converter is shown in Fig. 12. The local oscillator consists of a BF115 transistor TR_4 and a 41·666 MHz third overtone crystal. This third-overtone frequency is trebled by a BSX20 stage and amplified by a further BSX20.

A BF182 transistor TR_1 is used as an r.f. amplifier. This type gives good cross-modulation immunity at low on-tune signal levels, that is, when a.g.c. is not operating. The mixer comprises a BFS28 tetrode MOST TR_2 with signal injection on gate 1 and local oscillator injection on gate 2. A second BFS28 TR_3 is used as an i.f. amplifier to overcome the loss in the 100m length of coaxial cable from the converter to the receiver.

A typical power gain for the converter is 34dB and the noise figure is 5dB.

STATION OPERATION

The output power of the transmitter was adjusted to give 25W c.w. power directly after the aerial filter. The insertion loss of the 50Ω coaxial aerial feed cable was 4dB, thus giving a total radiated power of about 10W. The aerial gain was 12·6dB.

It may be noted that the maximum v.s.w.r. offered to the transmitter with a mismatched aerial would only be 2·2 so long as the coaxial feeder is connected.

The equipment was operated satisfactorily each weekday for about three weeks by qualified and licensed operators. Good quality transmitter signals were reported, mainly from South East England and, on occasions, North East England and the Netherlands.

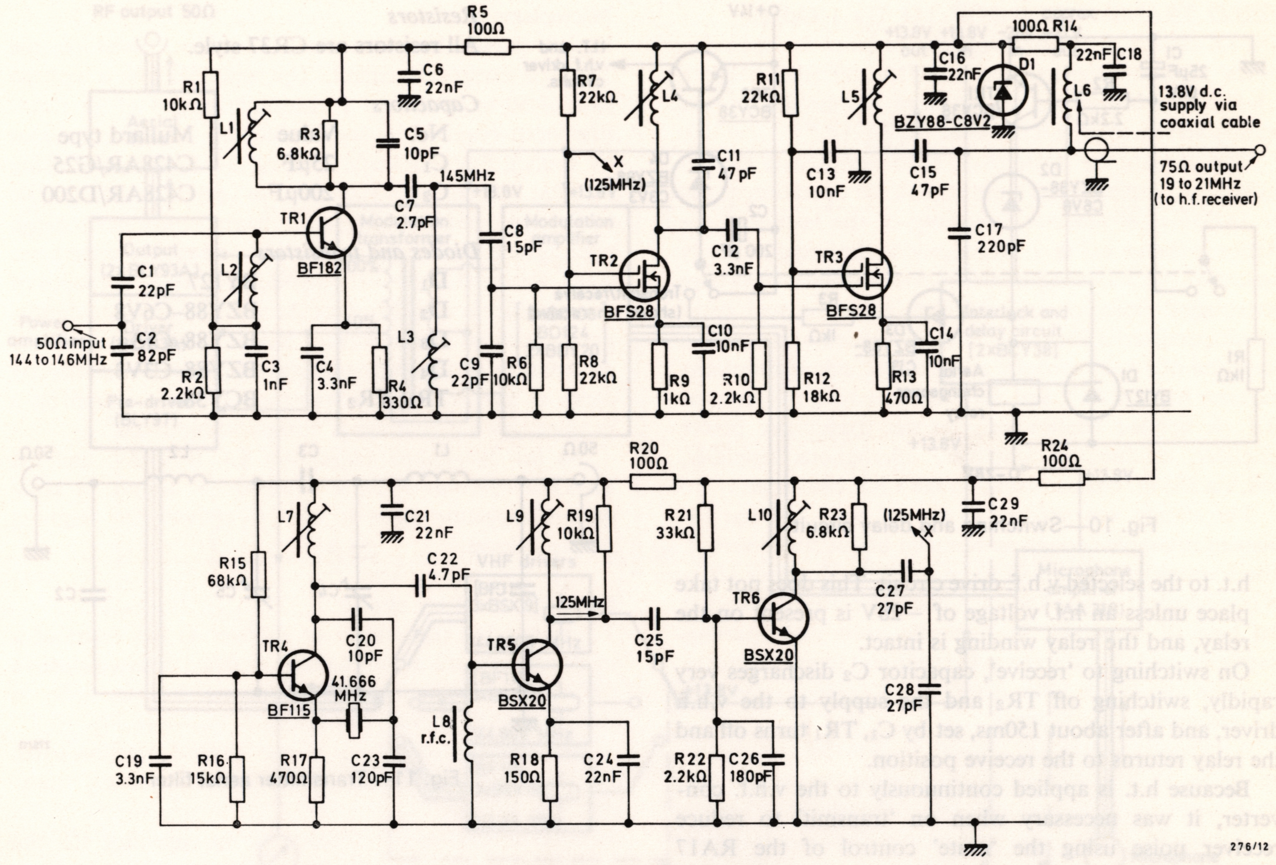
R5 100Ω
R1 10kΩ
C6 22nF
R3 6.8kΩ
C5 10pF
L1
145MHz
C7 2.7pF
TR1
BF182
C8 15pF
C1 22pF
L2
C2 82pF
50Ω input 144 to 146MHz
R2 2.2kΩ
C3 1nF
C4 3.3nF
R4 330Ω
L3
C9 22pF
R6 10kΩ
R7 22kΩ
(125MHz)
L4
R8 22kΩ
TR2
BFS28
C11 47pF
C12 3.3nF
R9 1kΩ
C10 10nF
R10 2.2kΩ
R11 22kΩ
C13 10nF
L5
TR3
BFS28
R12 18kΩ
R13 470Ω
C14 10nF
C16 22nF
BZY88-C8V2
D1
100Ω R14
22nF C18
L6
13.8V d.c. supply via coaxial cable
C15 47pF
C17 220pF
75Ω output 19 to 21MHz (to h.f. receiver)
R20 100Ω
R24 100Ω
L7
C21 22nF
R15 68kΩ
C22 4.7pF
L9
R19 10kΩ
R21 33kΩ
L10
R23 6.8kΩ
(125MHz)
C29 22nF
125MHz
C20 10pF
TR4
BF115
41.666 MHz
TR5
BSX20
C25 15pF
TR6
BSX20
C27 27pF
C28 27pF
L8 r.f.c.
C19 3.3nF
R16 15kΩ
R17 470Ω
C23 120pF
R18 150Ω
C24 22nF
R22 2.2kΩ
C26 180pF
276/12

Fig. 12—V.H.F. converter

Coil data

L_1, L_2, L_3, L_9, L_{10}	5 turns of 1·25mm enamelled copper wire, turn spacing 1mm, wound on a Neosid 4·5mm former with a Ferroxcube slug, grade 910
L_7	10 turns of 0·355mm enamelled copper wire, close wound on a Neosid 4·5mm former with a Ferroxcube slug, grade 910.
L_4, L_5	22 turns of 0·355mm enamelled copper wire, closewound on a Neosid 4·5mm former with a Ferroxcube slug, grade 900.
L_8	R.F.C. Painton type 200 509.

Resistors

All resistors are carbon film, style CR25.

Capacitors

No.	Value	Mullard type
C_1	22pF	C333CC/C22E
C_2	82pF	C333CC/C82E
C_3	1nF	630 02302
C_4	3·3nF	630 02332
C_5	10pF	C333CB/N10E
C_6	22nF	629 02223
C_7	2·7pF	C333CB/N2E7
C_8	15pF	C333CB/N15E
C_9	22pF	C333CC/C22E
C_{10}	10nF	629 02103
C_{11}	47pF polystyrene	
C_{12}	3·3nF	630 02332
C_{13}	10nF	629 02103
C_{14}	10nF	629 02103
C_{15}	47pF	C333CC/C47E
C_{16}	22nF	629 02223
C_{17}	220pF	C333CH/C220E
C_{18}	22nF	629 02223
C_{19}	3·3nF	630 02332
C_{20}	10pF	C333CB/N10E
C_{21}	22nF	629 02223
C_{22}	4·7pF	C333CB/N4E7
C_{23}	120pF	C333CC/C120
C_{24}	22nF	629 02223
C_{25}	15pF	C333CB/C15E
C_{26}	180pF	C333CH/C180E
C_{27}	27pF	C333CC/C27E
C_{28}	27pF	C333CC/C27E
C_{29}	22nF	629 02223

Transistors

TR_1	BF182	TR_4	BF115
TR_2, TR_3	BFS28	TR_5, TR_6	BSX20

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1. Cash, L. M., ‘VHF transistor transmitters for a.m. and f.m. operating directly from vehicle batteries’, **Mullard Technical Communications,** Vol. 10, No. 91, January 1968, pp. 2 to 13.

2 Prescott, M. J., ‘GB3MUL’, **Mullard Technical Communications,** Vol. 11, No. 109, January 1971, pp. 202 to 206.